Copper Electroplating and Mask-Free Techniques for Silicon Solar Cell Metallization

by

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ABSTRACT

This paper reports the results of studies comparing various patterning and electroplating methods for the deposition of Cu electrodes for silicon heterojunction solar cells, as well as developing and applying a novel mask-free plating process to plate copper patterns. The direct electroplating portion of this work compared the results of electroplating on different metal seeds from Ag, Ni, Cr and Ti by physical vapor deposition to the light induced plating of Ni/Cu directly on transparent conductive oxide. Patterning was performed using photoresists formed by spin-coating, screen printing or lamination. The geometry of the fingers, line resistance, contact resistance and adhesion were used as comparative parameters for the quality of the electroplated deposit on the different seed layers. The direct electroplating of Cu on the sputtered Ag seed achieved the lowest contact resistance and the best adhesion. All photoresists were able to achieve greater than 60μm resolution and could produce the fingers with the required height, despite the presence of mushrooming of plated copper. The most efficient silicon heterojunction cell with Cu contacts directly electroplated on the sputtered Ag seed achieved 21.9% efficiency on a 153cm^2 area. The localized electroplating process developed in this work produced definitive lines of plated copper without the use of any masking materials or methods on the cathode. Cu was deposited using this new method on polished brass substrates and polished silicon wafers with a sputtered Ag front coating, from anodes made of oxygen-free copper (OFC) and platinum. Plating applied voltage and anode-to-cathode distance are varied to study the effect on the plated lines profile. A full finite element method (FEM) model was created to simulate the growth of plated lines using different localized plating methods, including the method used in this work. The model was compared to measured

results and used as a predictive tool to simulate the effects of changing anode geometry for future applications in solar. Finally, non-ideal effects of the exposed wire anode plating were discussed, including variations in the electric field which lead to undesirable effects such as pillars, inconsistent aspect ratios, tapering and dendritic growth along the plated line.

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CHAPTER 1

INTRODUCTION

1.1 SILICON HETEROJUNCTION (SHJ) SOLAR CELLS

SHJ technology was developed as an independent cell structure to the industrial standard diffused junction (DJ) solar cell in 2001. The passivation qualities of the amorphous silicon (α-Si) heterojunction led to substantial improvements in efficiency and stability compared to the DJ cell. SHJ cells differ from an industrial standard DJ solar cells in Fig. 1-1.

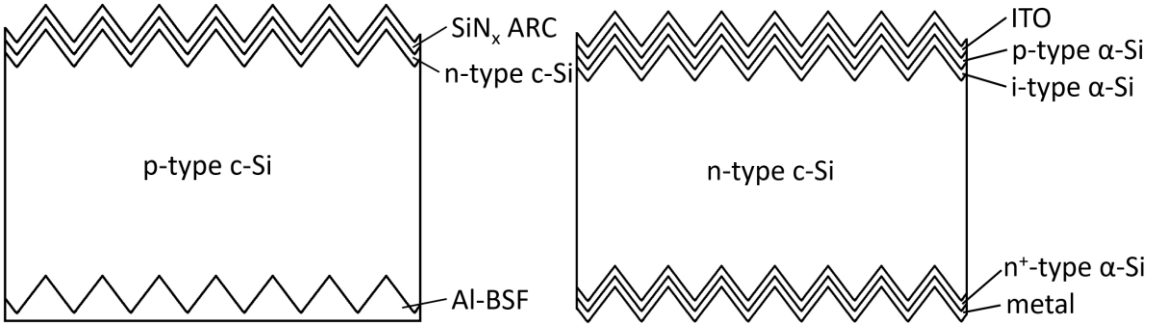

Fig. 1-1. Diagram of the cell structures of a (a) DJ solar cell and (b) SHJ solar cell.

To form an SHJ cell, amorphous silicon (α-Si) is deposited on a crystalline silicon (c-Si) substrate, in this work by means of plasma enhanced chemical vapor deposition (PECVD). The junction is formed between different doping of the amorphous layer to the crystalline substrate [1]. The α-Si also acts as a passivation layer for the c-Si substrate, which is why it is deposited on both sides of the substrate. First however, an intrinsic layer is deposited on the c-Si substrate before the junction is formed. While the need for this layer is not immediately clear, literature has shown this can mitigate stability losses of the heterojunction in the form of light induced degradation (LID) and reduce tunnelling, as well as supply superior passivation than just the p-type α-Si alone, increasing the fill factor

and efficiency of the SHJ cell [2]. Tunneling has been shown to occur between the p-type α-Si and the n-type c-Si due to the many localized states present in the doped layer.

The next layer deposited on the solar cell is the transparent conductive oxide (TCO). The reason for transparent conductive oxide (TCO) is threefold. The TCO is deposited onto the α-Si layer to minimize resistance for the transport of electron-hole pairs laterally to the fingers on the top surface of the solar cell. The α-Si layer is very resistive, and thus would contribute greatly to series resistance without the presence of a conductive top film. Secondly, the TCO passivates the top layer of the α-Si. Due to the nature of the TCO being on the front of the cell, it must also be transparent to a reasonable degree to allow photons to enter the cell. Therefore, the top surface cannot be covered with metal or some other conductive film. Transparency and conductivity in TCO films can be dial turned with different ratios of atomic elements however, they are inversely related. As such, carrier transport through TCO films should be limited to reduce overall resistance and maximize optical clarity. A metal front grid is still necessary to provide a more conductive path for carriers to leave the cell and provide energy for the load. A special, low temperature silver screen-printed paste is used to make electrical contact to the TCO and subsequently fired to solidify the paste. The TCO used exclusively in this work is Indium Tin Oxide (ITO).

The SHJ cell has remained remarkably like when it was first established, a testament to the robustness of the original design. Fig. 1-2 shows throughout the evolution of the SHJ cells, the technology has remained very similar in concept to initial designs. SHJ cells with a front grid resemble that of Fig. 1-1(b), while some designs, such as the high efficiency research cells have completely removed the front grid. The architecture of these cells in Fig. 1-2 are slightly different, taking on the name of interdigitated back contact (IBC) cells,

but may utilize the same heterojunction interface as the original. In fact, the current world record silicon solar cell efficiency is held by a SHJ IBC cell [3]. The most prominent are the full-size research SHJ cells from Panasonic, LONGi, and Kaneka, with conversion efficiencies of 25.6%, 26.5%, and 26.7% respectively [4], [5], [3].

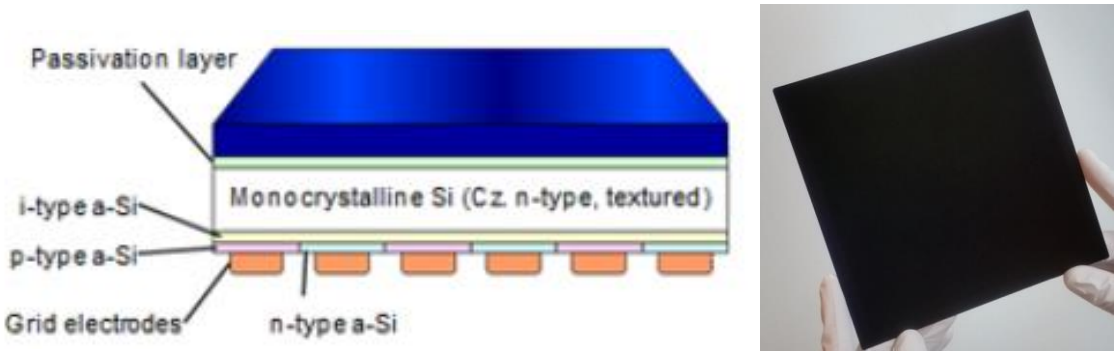

Fig. 1-2. One evolution of the SHJ solar cell. The front grid has moved completely to the rear of the cell to maximize light entering the cell. The back layout has an array of interspersed n and p layers. Photo credit: Photovoltaic & Thin Film Research Laboratories (Kaneka corporation).

SHJ cells have held the world record of efficiency for silicon solar cells for many years, which has kept this cell type holding a smaller, but not insignificant 15% of production market share projections by 2030 [6]. Some of the largest issues with mass production include front metallization, extensive use of vacuum tools and in complex processing. Additionally, the current front metallization scheme with the low temperature Ag screen-printed paste limits the potential of SHJ cells by means of increased series resistance. However, due to the conductive nature of the front side TCO unique to SHJ cells, it is compatible with a metallization technology such as electroplating, a core concept of this work. Electrical contact can be made to the TCO, whereas the insulating SiN_x on the surface of the DJ cell cannot be electrically contacted. Fig. 1-3 shows the metallization differences between the traditional screen-printed front grid and the process of integrating

of an electroplated front grid for an SHJ cell. By applying an intermediate layer, in this work referred to as a “seed” layer, that is compatible with both the TCO and the electroplated metal, it is possible to electroplate that metal onto the solar cell. Different seed layers have been observed in literature, some more successful than others. Kaneka demonstrated a large area Cu-SHJ cell on a vacuum deposited seed layer with 25.1% efficiency, which held the world record among both sides contacted silicon solar cells in 2015 [7]. High efficiencies above 22% on Cu-SHJ cells were also reported by other labs using various seed layers in 2015 [8], [9], [10], [11]. In 2014, Silevo became the first company providing PV modules based on Cu-SHJ technology on commercial basis with a proprietary seed layer. There are many benefits to replacing the screen-printed Ag paste with electroplated metals as the front grid of the SHJ cell and they are explored in this work. The seed layer combined with electroplating requires two new processing steps that are not standard in a typical solar pilot line. Vacuum sputtering/evaporating are used in this work to deposit the seed layers, and the SHJ cells are submerged in electroplating solution to deposit the front grid. Conveniently, since the ITO is deposited in a vacuum deposition step immediately prior to the seed layer deposition, it is a simple measure of placing an additional metal target in the vacuum deposition tool. In short, the seed layer and TCO can be deposited without breaking vacuum, which saves on time and cost. The final aspect of the integration into SHJ cell structure is the electroplating step itself. Electroplating baths and masking steps are required to define the front grid which historically, tends to be costly when using traditional methods such as photolithography. The electroplated metal, which in this work is Cu, is more conductive than the screen-printed Ag and cheaper than the bulk material price of Ag. Silicon heterojunction solar cells with Cu front grids deposited by

electrochemical plating (Cu-SHJ) have been shown to reduce levelized manufacturing costs associated with the increase the efficiency of PV modules [12], [13]. If the electroplating masking process can be made more cost effective, an electroplated front grid would mark a significant step towards competitive production with industrial standard DJ technology.

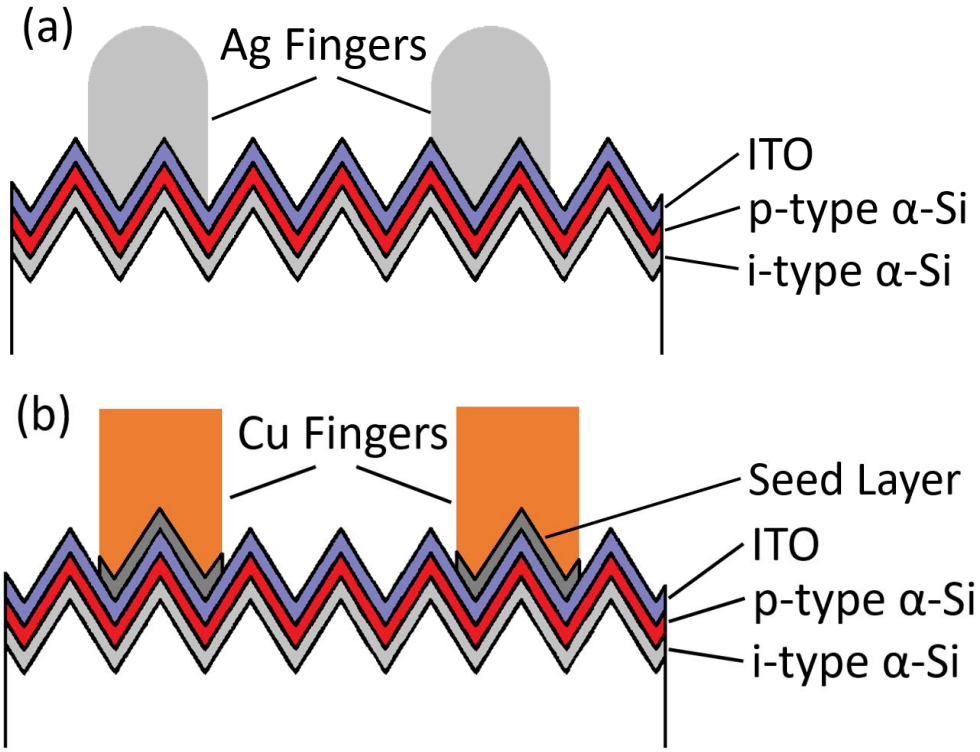

Fig. 1-3. SHJ cell structures with (a) screen-printed fingers and with (b) Cu plated fingers. Due to the deposition method and possible material incompatibilities, it is necessary to include an intermediate layer between the Cu and ITO, labelled in (b) as the Seed Layer. Several materials are explored in this work as compatible Seed Layers.

1.2 TUNNEL OXIDE PASSIVATED CONTACT (TOPCON) SOLAR CELLS

TOPCon solar cells are the potential successor to the original DJ, Passivated Emitter Rear Contact (PERC) and n-Passivated Emitter Rear Totally diffused (n-PERT) solar cells composing the majority of market share of solar cells the last 20 years. TOPCon solar cells

were introduced by Fraunhofer in 2013 as a progressive technology to advance current industrial scale solar designs [14]. TOPCon, like PERC cells, are composed of the basic DJ cells structure with a several design changes that improve cell efficiency. Such designs are useful for industry, as they require little modifications to existing pilot lines for integration into full scale production [15]. Because of this, industrial cell results can be reported in a relatively short turnaround time [16]. As seen in Fig. 1-4, the major cell changes from the DJ line occur in the passivation and transport mechanisms on the rear of the cell. The presence of a thin, SiO_x film between the metal and the Si forces carriers to quantum mechanically tunnel to the rear contact from the c-Si bulk, vastly reducing the recombination current density at the rear of the cell, among other benefits [14]. The front of the cell, where this work is focused, changes little conceptually across technologies. The DJ structure utilizes a monocrystalline silicon wafer that undergoes a diffusion process of opposite dopants on the front of the cell to form the junction whereas for TOPCon, researchers have explored junctions created with diffusion as well as with ion implantation [17]. In Fig. 1-4, the DJ cell in (a) would undergo a n-type dopant diffusion process while the TOPCon cell in (b) would undergo a p-type dopant diffusion process or ion implantation. For a DJ cell, the front surface is passivated with a non-stoichiometric silicon nitride (SiN_x) deposited using Plasma Enhanced Chemical Vapor Deposition (PECVD) that functions primarily as an anti-reflection coating (ARC). The front passivation is more optimized in a TOPCon cell, typically incorporating a double layer ARC. Multi-layer ARCs are used to further decrease reflectance of various wavelengths of light compared to single layer ARCs, with more ARC layers increasing the amount of absorbed light in the silicon bulk [18]. While silicon nitride has been used to passivate the n-type emitter of DJ

cells, TOPCon's deviation to superior performance n-type silicon wafers requires a more optimized film to properly passivate the p-type emitter. Built in positive charges in commonly used passivation films such as silicon nitride and oxide lead to a poorer passivation on p-type silicon than a film with built in negative charges such as aluminum oxide [19]. Thus, the p-type emitter is passivated with an atomic layer deposition (ALD) AlO_y, followed by deposition of the SiN_x layer to be used as the second stage of the ARC.

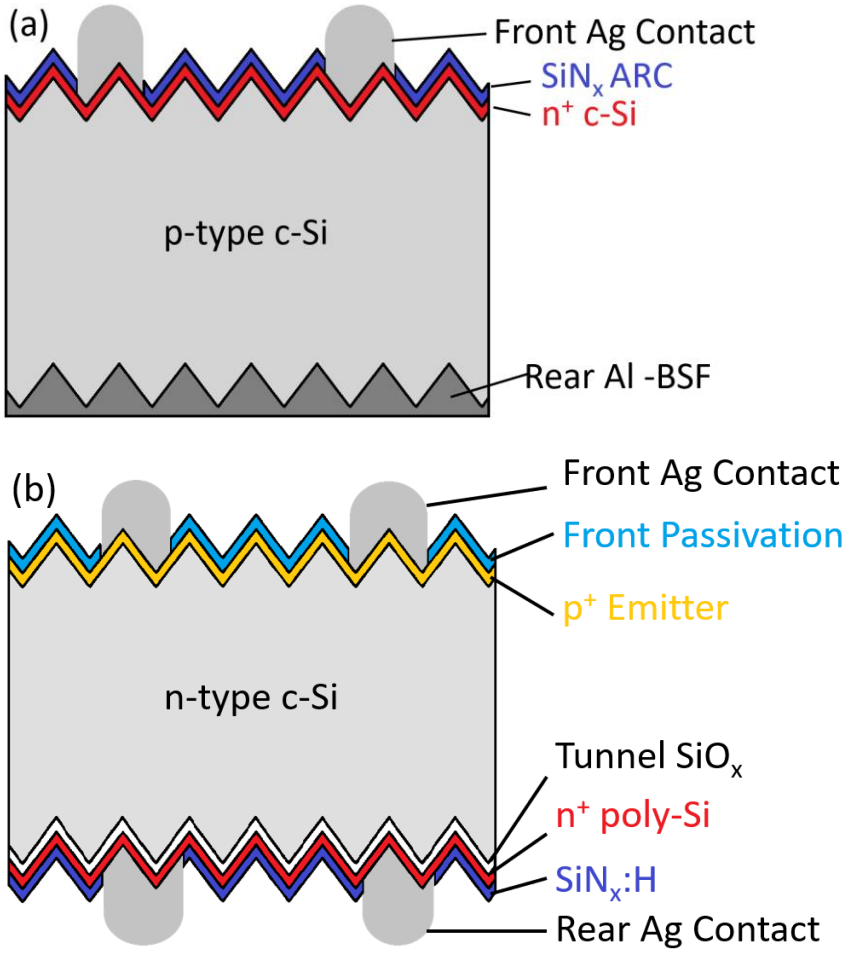

Fig. 1-4. Cross section diagrams of (a) a traditional DJ solar cell with front screen-printed Ag contacts and rear fired Al-BSF and (b) proposed TOPCon structure which includes rear side passivation separate from the grid contacts. In both cases, front and rear metal is fired through the existing passivation layers to contact the c-Si substrate (poly-Si in the case of TOPCon rear contacts).

Excluding rear surface formation, the next step after the deposition of the ARC layers on the front surface is the front metallization process. DJ and TOPCon cells must utilize screen-printed silver paste to make contact to the emitter. The paste is deposited directly onto the ARC layers and fired. The firing process drives the silver paste through the ARC and passivation layers and makes electrical contact to the emitter. The ARCs are electrically insulating, so the metallization layer needs to penetrate the ARC to make good ohmic contact to the doped c-Si underneath.

The insulating SiN_x in the DJ and consequently, the TOPCon structure, presents challenges for electroplating. Being an insulator, it is difficult to sufficiently charge the front of the solar cell to allow for copper electroplating to occur. A metal seed layer, such as the one presented in Section 1.1, would make the front of the solar cell more conductive for plating, but ohmic contact would not be made to the silicon surface due to the intermediate layer of insulating nitride. As such, electroplating is not immediately integrable for TOPCon structures. However, future ARCs, electroplating combinations with other technologies such as multiwire, advancements in the technology proposed in this work, changes in the TOPCon structure, among others, have the potential to fully incorporate electroplating contacts with the TOPCon solar cell [20]. Despite this, research groups are still reporting TOPCon cell structures with copper electroplated front grids, just as there were numerous attempts to create electroplated front grids on DJ solar cells [21], [22]. Also, the TOPCon structure is expected to overtake PERC and become the dominant cell technology by 2030, making this cell structure extremely relevant to study [6]. Due to the benefits of a copper electroplated front grid outweighing the difficulties of incorporating one, in addition to the importance of TOPCon cell technology and the

corresponding market share, it is safe to assume the electroplating technology will eventually be integrated in some way to the TOPCon structure.

1.3 SILVER SCREEN PRINTED TECHNIQUE

The dominant front metallization technique for DJ solar cells is the Ag screen-printing technique. The deposition process is similar to how images are printed on T-shirts, and first-generation solar cell Ag screen printers were simply modified T-shirt printers as in Fig. 1-5(a). First, Ag paste is placed onto a screen made of metal mesh. The mesh in Fig. 1-5(b) is open in regions where paste needs to exit. A solar cell is placed under the mesh and a squeegee is run over the screen with a certain pressure. As shown in Fig. 1-5(c) the squeegee drags the paste over the entirety of the mesh and paste is allowed through the regions of the mesh that are clear. In this way, a solar cell grid pattern is applied onto the front of the solar cell.

Silver itself is a solid at room temperature, and to make an emulsion that is screen-printable, organic compounds of various quantities and types are added, depending on the rheological properties needed for the application. Other additives are present such as glass and lead frit but are used to bind the Ag to the solar cell [23], [24]. To solidify the paste to make final electrical contact possible, it must be dried and fired at temperatures around 800C. The purpose for drying and firing is twofold: the outgassing of the organic additives to solidify the Ag paste and the penetration of the Ag contact through insulating SiN_x layer. The organic compounds in the paste evaporate, leaving a porous Ag front grid making ohmic contact to the front of the cell and the glass frit penetrates through the dielectric SiN_x layer, allowing the Ag to make ohmic contact to the c-Si.

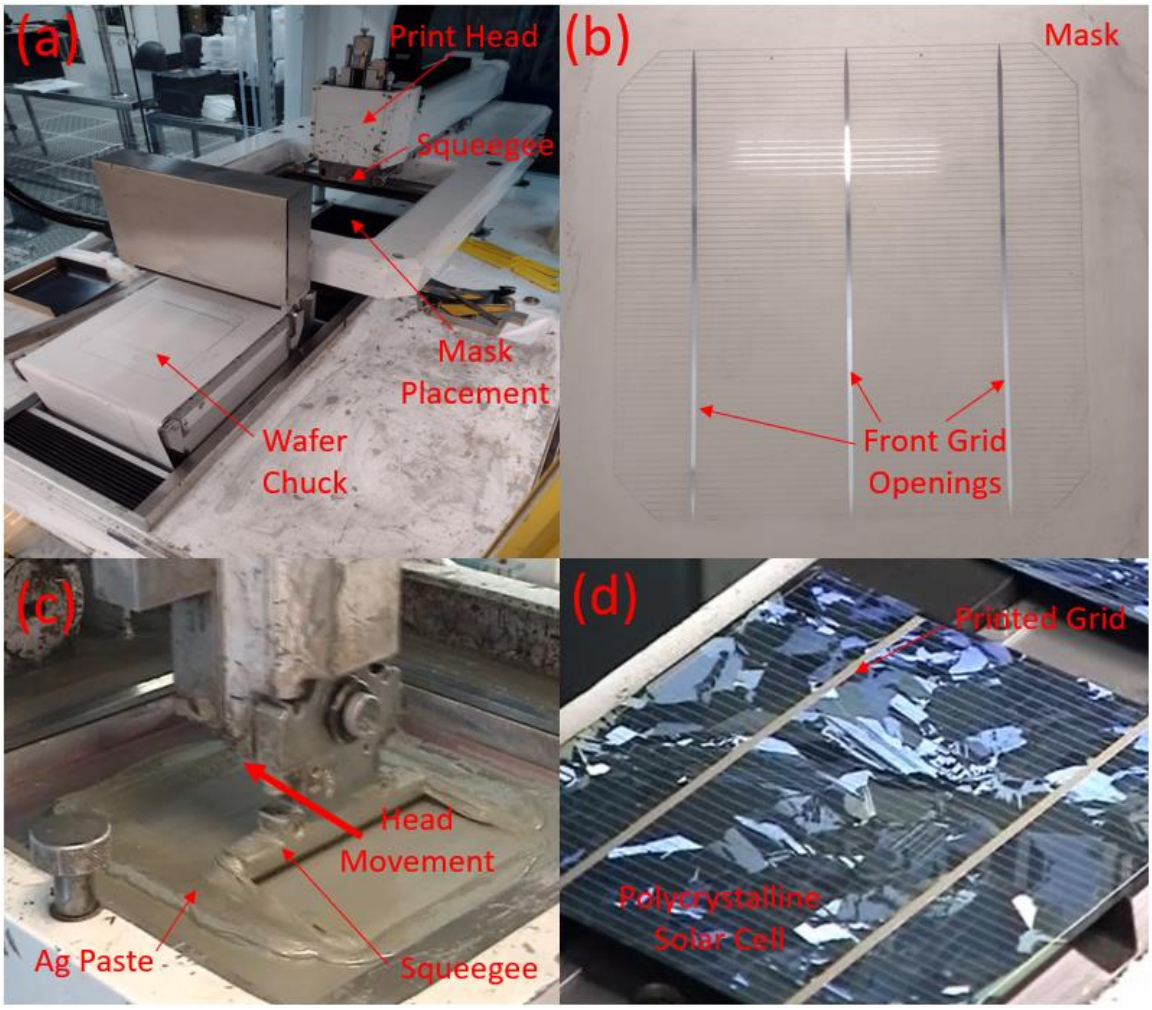

Fig. 1-5. General processing and materials for screen-printing a solar cell. (a) Modern automated screen printer with corresponding parts and (b) a screen-printing mask designed to print a 3BB pattern with 60um fingers. (c) Industrial screen-printer squeegeeing Ag paste through a 2BB mask on a (d) polycrystalline solar cell manufacturing line. (c) and (d) courtesy of [25].

For SHJ cells, the presence of the temperature sensitive α-Si limits the firing temperatures to 200°C since annealing temperatures beyond 200°C have been shown to decrease the photovoltaic properties of SHJ cells by means of out diffusion of hydrogen in the α-Si layers. The loss of the passivating hydrogen increases the defect density at the α-Si/c-Si interface and lowers minority carrier lifetime, in addition to compensating the doping in the α-Si [26]. This irreversibly destroys the benefits reaped with the amorphous

heterojunction structure. Therefore, a special low-temperature paste was developed for the specific application of SHJ cells. The paste is a derivation of the traditional silver screen-printed paste used for diffused junction cells but is instead resin bonded and cured to the SHJ cell [27]. The conductive resin contains flakes of Ag that are much larger than the nanoparticles in fired paste. The flakes leave much larger gaps than the nanoparticles between Ag pieces, leading to overall increased resistivity of the front grid, but the curing temperature is reduced to ~150C from 800C in traditional pastes [28]. Additionally, there is no dielectric ARC on the top of the SHJ cells. A conductive TCO is present, meaning the paste makes ohmic contact directly to the top surface of the solar cell. The high resistivity of this front grid offsets several advantages of SHJ cells over DJ cells, but for years it was the only front metallization available for SHJ cells, until the arrival of other low temperature metallization techniques such as Cu electroplating were adapted for solar cell use.

1.4 TRUE COST OF SILVER PV INTEGRATION

Silver is a valuable commodity with importance in many industries, such as its use as an antibiotic in medicine and a conductive material in electronics, solar being no different. Besides its practical usefulness, silver is a precious metal that is used in most countries as an investment or as a hedge against inflation. As such, the price of silver tends to wax and wane with the economies of the world, and most significantly with the United States. Fig. 1-6 shows the volatility of the price of silver and copper in the past 50 years. Copper is also examined since bulk copper prices are directly correlated with variable costs associated with electroplating systems such as the electrolyte cost. While copper experiences some volatility relative to itself, it is important to note how the price of copper never exceeds

silver, nor does the price change in magnitude as much as silver. Also, the price of bulk silver varies anywhere between 100x-300x the price of bulk copper. At the lowest price point, silver is a necessary expense to achieve the conductivity required for an industrial silicon solar cell front grid, and at the highest price, silver becomes a luxury only the more established manufacturers can afford. With the price of silver currently over $600/kg, the metallization of the front silver contact alone is over 25% of the cell cost for an industrial standard monocrystalline PERC cell with 22% efficiency [6].

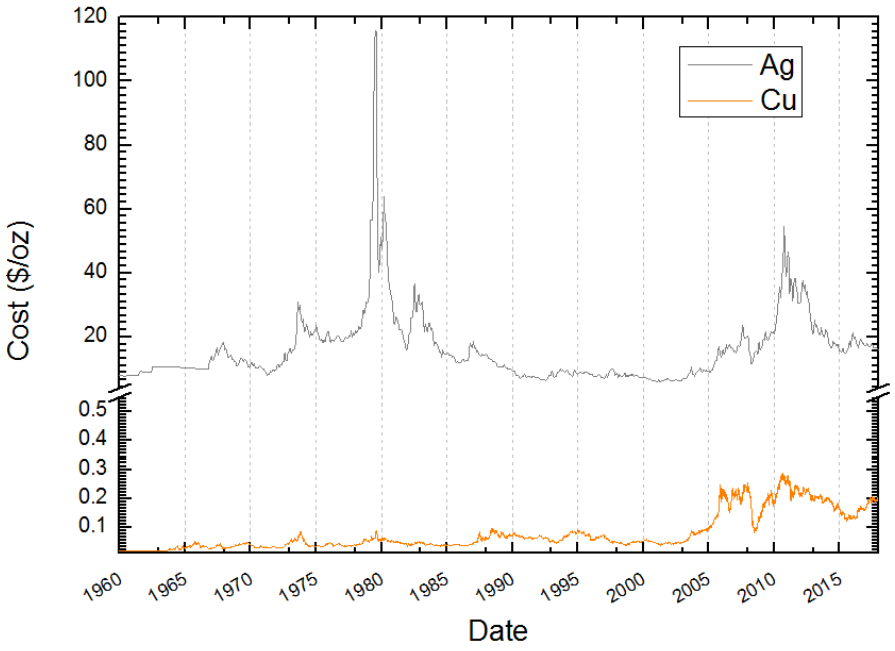

Fig. 1-6. Inflation-adjusted bulk price of Ag and Cu in US dollars dating back to 1960. Data extrapolated from [29], [30].

In addition to price volatility, silver is not a sustainable resource and photovoltaic module recycling will be crucial to reclaim silver necessary to achieve worldwide Terawatt-scale deployment. This is especially important since future cell production capacities by 2030 are predicted to consume roughly 8000 tons of silver per year, about one-third of the world's annual production at that time [31]. As shown in Fig. 1-7,

photovoltaics (PV) production in 2017 utilized 10% of the world's annual silver production in that same year. Due to high demand of silver and the amount in current reserves, it would be impossible to achieve terawatt-scale deployment for PV. The entirety of the world's silver reserve amounts to 530,000 metric tons, according to the mineral commodity summaries published by U.S. Geological Survey in 2022 [32]. Contrast the silver scarcity with copper, which is not a precious metal. Current world reserves of copper amount to 2.1 billion metric tons, with an estimated 3.5 billion tons of undiscovered copper in the Earth's crust [32]. Assuming all future solar cells manufactured follow a standard 7 W DJ solar cell with 7% front metallization coverage and 12um tall front grid, the world's reserve of silver will be depleted producing solar cells powering only 5% of the 46TW power supply needed by the United States in 2100 [33], [34].

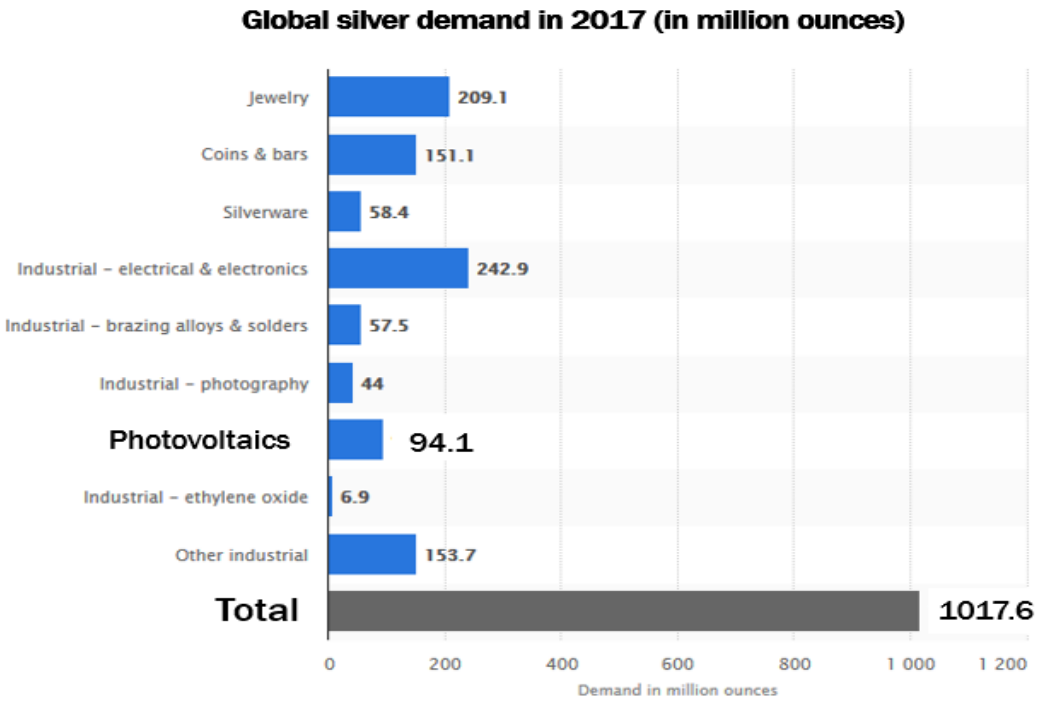

Fig. 1-7. Total global silver demand in grey and piecewise components labelled in blue for 2017. Chart used from [35].

The volatile price of silver combined with the resource constraints leads to an unreliable and unsustainable future of silver screen-printed solar cells, despite intentions to reduce silver consumption per cell. This work introduces methods for copper front grid metallization to fully replace silver screen-printing. In addition to being cheaper and significantly more abundant, Cu has already been implemented in research solar cells and provides other benefits that will be discussed in this work.

1.5 OVERVIEW OF COPPER ELECTROPLATING

Electroplating is the process of depositing a metal onto an object using an electric potential in a liquid electrolyte. This work focuses on the deposition of copper, so any reference to electroplating, unless otherwise specified, will refer to an acid copper sulfate-based electrolytic bath. In the most elementary form of electroplating, an anode made of high purity oxygen-free copper (OFC) with phosphorous additives is submerged in a copper electrolyte, sulfuric acid-based bath with a cathode comprising of an appropriate metal. The bath can be various temperatures which affect plating rates, but acid-copper baths can achieve sufficiently high plating densities compared to other chemistries at room temperature, which made the exotic fixtures necessary for this work simpler to design, since no heating element was present. Additionally, the room temperature deposition makes Cu electroplating compatible with the low temperature processing requirements of SHJ cells.

In general electroplating, the anode is electrically connected to the positive terminal while the cathode is negative as seen in Fig. 1-8. Copper sulfate is soluble in water, so it dissociates into Cu^{2+} and SO_4^{2-}, which compose the electrolyte. The now free Cu^{2+} become hydrated and diffuses toward the cathode. To simplify the example, the necessary forced

flow of ions in what is known as convection is ignored. The hydrated Cu^{2+} cations are not able to bond to the cathode in a region close to the cathode known as the diffusion boundary layer, without first shedding the hydration shells surrounding the cations [36].

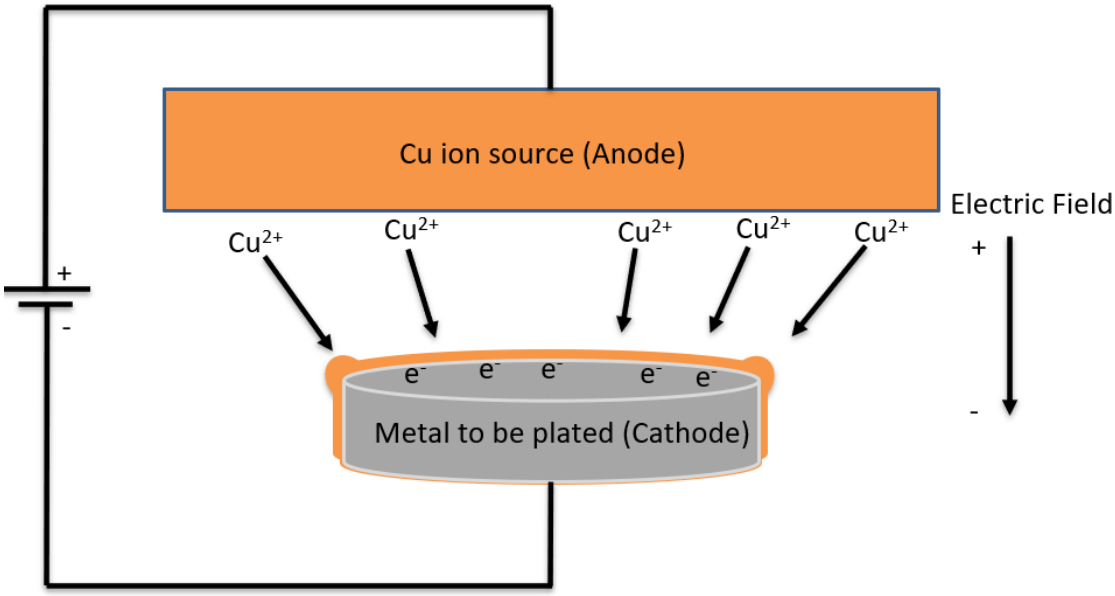

Fig. 1-8. Simplified diagram of industrial copper electroplating process. The electric field from the power supply drives copper ions from the anode to the cathode. The anode is a source of purified copper, and the cathode can be any metallic or conductive material.

The activation energy required is supplied by the external power supply, and the Cu^{2+} cations become bound as adatoms to the cathode surface, where they migrate to energetically favorable sites and permanently bind to the crystal structure. Sulfate ions move the opposite direction in solution and bond with the bulk copper of the anode where they form $CuSO_4$ in solution, which then dissociates into an electrolyte, beginning the cycle again. The copper formed on the cathode is very pure and dense, meaning the conductivity of the deposited copper rivals that of bulk copper. In fact, the conductivity of as-deposited electroplated copper can be as much as 3x higher than the best Ag pastes on the market [37]. The density is dependent on several factors that are discussed in this work, but there

are very few limiting factors for the upper limit on electroplated copper density. Since the electroplated copper forms by electric field driven adatom bonding, there is a possibility for very high density and very few gaps, or pores in the resulting plated structure. Previous work by Lennon et al. in Fig. 1-9 shows the cross section of a plated Cu line compared with a cross section of in-house screen-printed Ag line [22]. The Cu resembles that of a bulk semicrystalline material, as the grain lines are clearly visible and no obvious holes in the plated line are present, whereas the screen-printed Ag line resembles a formation of droplets with a close-up image showing vast number of micropores in the structure.

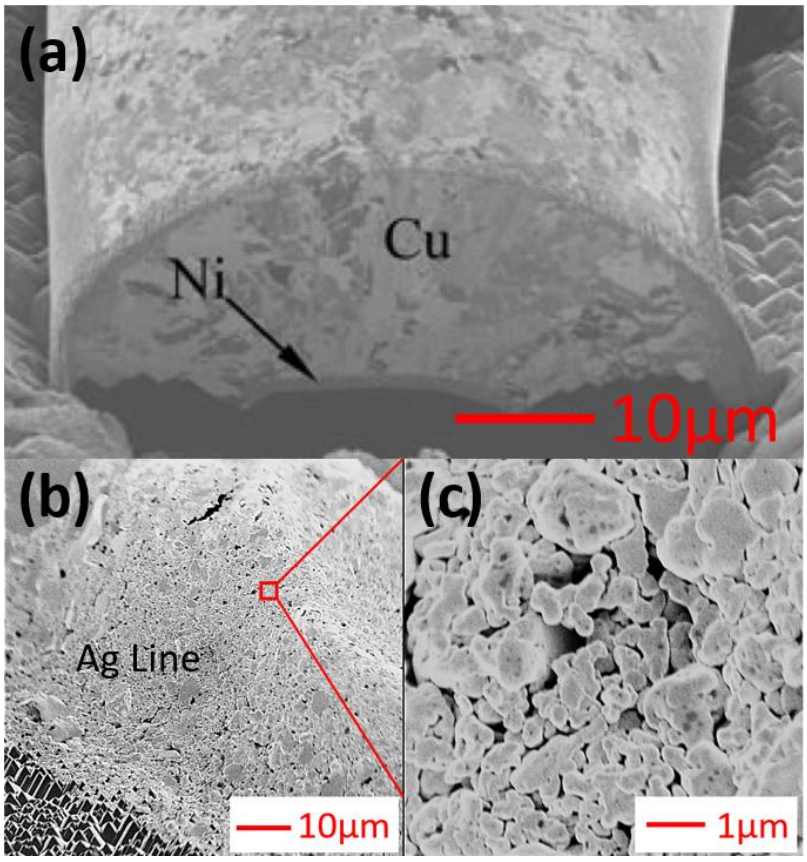

Fig. 1-9. SEM images of a (a) cross section view of an electroplated Cu line on a Ni seed layer and (b) a silver screen-printed line viewed adjacent to the line. Images are from (a) Lennon et al [22] and (b)-(c) an ASU DJ solar cell.

Deposition temperature as well as thermal and mechanical stress also becomes a factor as cell manufacturing progresses. It has already been shown that the high heat involved with soldering ribbons to the front grid of solar cells causes microcracks in the cell near the ribbon [38]. Even processes that undergo "low temperature" bonding such as ultrasonic welding for front ribbons still require temperatures around 200C to bond to the Ag front grid [39]. The Ag screen-printed front grid is no different in this regard. The expansion and contraction of the front grid Ag at 200C places enormous stress on the solar cell. This internal stress is a result of the coefficient of thermal expansion of the different materials being bonded. The Ag honeycomb has a 10x larger thermal expansion coefficient than bulk silicon, so when the wafer is cooled after firing, the Ag front metal will shrink much more than the wafer, leading to internal stresses which can cause solar cell breakage in extreme cases. According to the ITRPV, the price of silicon and the push for lower cost per cell will continuously drive solar cells thinner [6]. Thermal stress will only worsen with thinner cell design, as there is less silicon bulk to resist the bowing of the metal grid when firing [40]. It is important then, to adopt metallization techniques to reduce this damage as cell yield may become affected. Electroplated copper offers a solution to this problem: since copper is electrodeposited at room temperature, the main stress that is applied to the solar cell is mechanical. Even though the thermal expansion coefficient of Cu is approximately the same as Ag, the deposition ideally occurs the same temperature the cell will be operating in, so little thermal stress is applied over the life of the cell. Fig. 1-10 shows how deposition stress is affected by each metallization technique. Stress occurs when the Cu is deposited and as it grows during electroplating, as well as after electroplating. Electroplated Cu self-anneals at room temperature and changes crystallinity in a period of hours to days, with

grain size typically increasing with time [41]. The annealing rates and crystal sizes are mostly determined by the electroplating parameters of the bath and substrate during deposition [42]. While no quantitative measure of bow was taken for this work, Cu and Ag 140um thick solar cells were compared on a polished granite stone with a precision flatness and surface roughness. The cell with the Ag front grid had a noticeable bow whereas the Cu cell did not. However, a cell that was 20um thick with Cu electroplated front contacts was created during this work as an extracurricular, and it was found to create a noticeable bow on the cell. As predicted, there is a lower limit on cell thickness for Cu front contact solar cells. How much bow is acceptable to maintain high yields during mass production is beyond the scope of this work. Bow and stress are used as a simple metric of comparison between front metallization technologies and applications for SHJ and TOPCon solar cells.

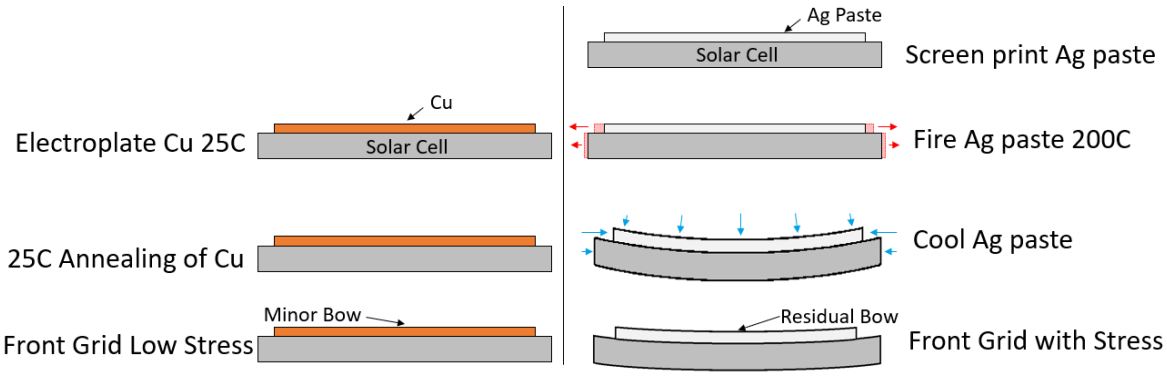

Fig. 1-10. Deposition stress of Cu and screen-printed Ag. Cu stress is minimal and not shown but is still present on the wafer. Just as with Ag, Cu stress would be more visible as wafers become thinner. Cu stress is also a function of electroplating parameters. Different plating rates, bath temperatures, etc. affect post-deposition annealing of Cu and thus have varying bow intensities. When cooling the Ag front grid after firing, bow is at a maximum due to the now bonded Ag and silicon wafer. Cooling begins on the outer edges and moves inward leading to slight relaxation of the wafer and front grid.

Copper electroplating front grids has been proposed as an economically and sustainable alternative to the silver screen printed paste for the front grids of solar cells displayed in

Section 1.4. Copper is more abundant and cheaper than silver, and the near-pure metal deposition of electroplating translates to a higher conductivity than the Ag paste. These advantages, coupled with room temperature deposition, provide a desirable metallization scheme for SHJ and TOPCon solar cells.

1.5.1 COPPER ELECTROPLATING IN SOLAR RESEARCH

There are several key barriers to integrating copper electroplating into solar pilot lines. Arguably, the most important is the isolation of copper from the silicon bulk. Copper is a deep-level trap in silicon and is extremely mobile in the crystalline bulk, even at room temperature [43], [44], [45]. Copper deposited on the front of a bare silicon solar wafer could interstitially diffuse to the rear of the cell in a matter of minutes, and if present in the space charge region, would short the p-n junction of the solar cell. At best this would reduce the efficiency of the cell and at worst it would lead to complete cell failure in a module. Thus, it is critical that copper be deposited on a layer that copper cannot migrate through, termed a “diffusion barrier” to protect the silicon bulk. This layer would need to be compatible with the solar cell structure so that gains from using copper are not offset by losses incurred by the diffusion barrier layer. The second issue is the necessity of a mask layer for the front grid. Electroplating is a non-selective deposition process, and thus plating would occur anywhere a ground potential exists on the solar cell. A mask can take many forms such as a physical barrier placed on the solar cell to prevent the electrolyte from flowing onto areas of the wafer not formed by the front grid, or a preferential chemical grow point placed on the cell, such as in electroless plating [46], [47]. These and all subcategories are considered masked methods because they are either masks themselves, they need to be placed on the solar cell using a mask, or some patterning step is involved

with the formation of these masks [48], [49], [50], [51]. A review of masking methods and dielectric masks can be found elsewhere [52], [53]. Some of the more pursued masking methods are photolithography and oxide/nitride chemical vapor deposited (CVD) layers [54], [55]. Both methods are shown in Fig. 1-11.

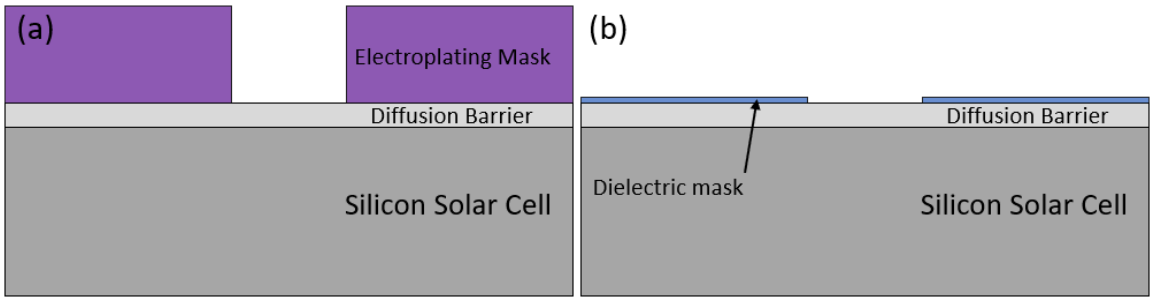

Fig. 1-11. (a) Photolithographic mask and a (b) nitride/oxide mask deposited on a solar cell to guide electroplating. Mask scales in (a) and (b) are relative to each other. Random pyramid structure on the silicon is not shown for simplicity.

Dielectric masks are deposited via some form of CVD, followed by laser ablation of a front grid pattern. The underlying cell is exposed to the copper electrolyte, so copper will preferentially plate to the charged, exposed regions of the solar cell rather than the top insulating dielectric layer. However, the dielectric layer is very thin, typically around 100nm. Such a thin layer is difficult to conformally deposit, so pinholes are present which can lead to “ghost plating,” or spots where copper is deposited, but doesn’t contribute to current extraction from the cell. Additionally, in Fig. 1-12(b), there is no guide for plating, i.e., copper will plate isotropically outward, which limits the extent of plating on the cell, as lateral growth leads to shading and reduction of solar cell current. Photoresist, a much thicker mask on the scale of 20μm is more physically suited to the front grid construction of solar cells. The rectangular profiles exhibited with high quality photoresist lead to higher aspect ratio copper structures than that of an oxide/nitride layer. As seen in Fig. 1-12(a),

parasitic shading would not occur with photoresist plated structures since plating is only conducted vertically within the walls of the photoresist.

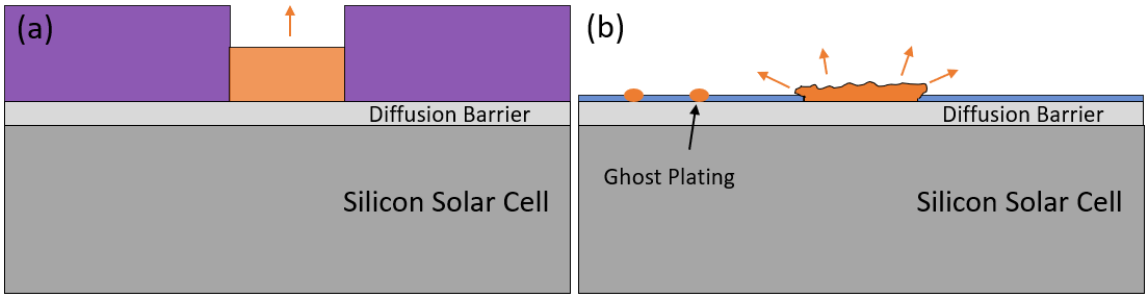

Fig. 1-12. Arrows show copper growth directions in (a) photolithographic mask channel and out of a (b) dielectric mask. (b) Dielectric masks are thin enough to develop pinholes that lead to ghost plating.

There are several methods of electroplating copper to solar cells. The two main methods discussed in this work will be contact electroplating and light-induced plating (LIP). Either can be used to create a full front grid, but this work focuses on contact electroplating to make the full front grid, while LIP is used to create a test seed layer. Another method of electroplating known as localized electro-chemical deposition (LECD) has previously been used to create complex 3D microstructures on copper substrates but has not been used in solar applications [56]. This work also explores a novel variant of LECD, developed and named in this work wire-LECD (WLECD), as a future application of LECD to solar cell metallization schemes.

Table 1-1 summarizes plating technologies reported in literature for Cu-SHJ solar cells with a front grid in the last several years. The best results were achieved by Kaneka and Silevo, which use EP on a physical vapor deposited (PVD) metal seed patterned by photoresist with the subsequent etching of the seed. This method requires making a direct contact to the sputtered seed to supply current with a corresponding wafer holder and

plating tool design. In the alternative method being developed by for example, Meyer Burger, CSEM and UNSW, a Ni/Cu stack is deposited on a patterned ITO using LIP.

Table 1-1. A review of the best Cu electroplated SHJ cells reported in literature.

Lab	Plating Method	Patterning Method	Minimum finger width (µm)	Area (cm^2)	Reported Efficiency (%)
Kaneka [7]	Electroplating on PVD seed	n/a	30-40	152	25.1
Silevo [10]	Electroplating on PVD seed	Dry photoresist film	32	239	23.1
CSEM [9]	Ni/Cu light induced plating	Inkjet of hot-melt resist	15	4	22.4
Meyer Burger [8]	Ni/Cu light induced plating	Inkjet of hot-melt resist	35	152	22.3
SIMIT [11]	Cu on IWO	Photoresist	53	n/a	22
SERIS [51]	Ni/Cu light induced plating	Screen print resist mask	80	4	19.1
UNSW [57]	Cu light induced plating with adhesion promoter	Inkjet lithography	20	239	18.8
Typical industrial screen-printed Ag SHJ cell				153/239	20-22
ASU screen printed Ag SHJ cell				100	21.5

CHAPTER 2

DIRECT CONTACT ELECTROPLATING FOR SHJ SOLAR CELLS

In the simplest form, contact electroplating for solar cells follows most closely a standard integrated circuit (IC) electroplating process as seen in Fig. 2-1. However, challenges arise when a solar cell, instead of a metal, is used as the cathode in the electrochemical cell. Electrical contact, proper adhesion layers, and proper materials compatibility are some of the issues that are discussed in this work and arise from the integration of copper. The solar cells used in this work do not exceed 160μm in thickness, meaning electrical contact is limited to the front or back of the cells and not the sides. Since metallization is one of the final steps in cell production, the p-n junction has already been formed on the wafer. Electrical contact on the back of the wafer would provide the benefit of isolating the rear

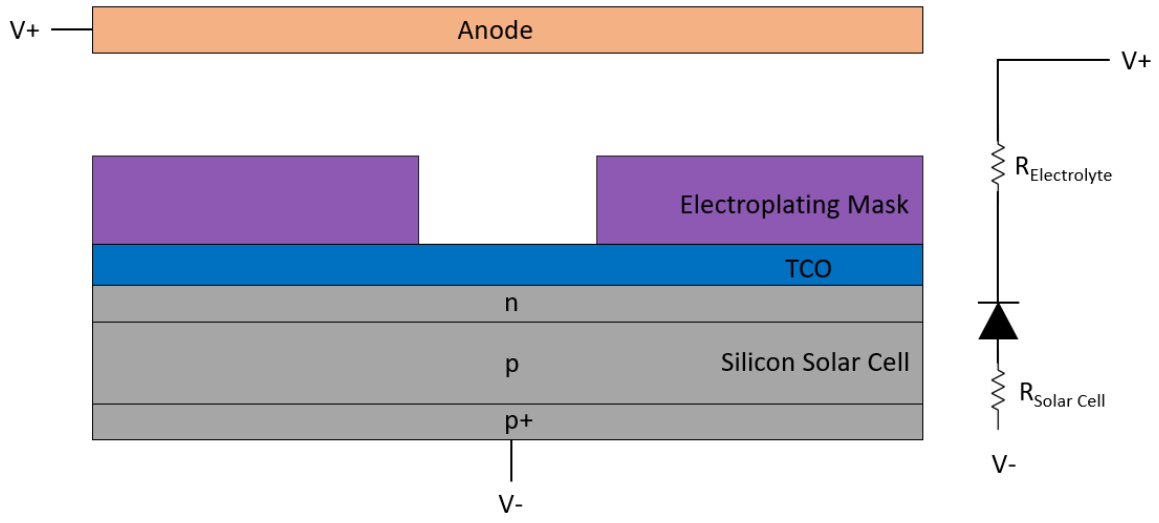

Fig. 2-1. Simplified electrochemical diagram of a solar cell with a p-type bulk and rear-contacted where $R_{Electrolyte}$ includes bath and electrode capacitances and resistances. The circuit diagram shows the diode configuration of solar cell when the positive potential is applied to the anode. An n-type wafer would reverse the diode and prevent current from flowing in the electrochemical system. An infinite shunt resistance for the solar cells is assumed here since shunts are considered imperfections and not intentionally implemented in solar cell processing.

of the cell and the electrical contacts from the solution. This is a simple method to avoid parasitic plating to the electrical contacts. But, depending on the cell design, being n-type or p-type, it is possible that electrochemical current entering from the rear of the cell will be halted altogether from the wrong facing junction if the cell is back contacted as in Fig. 2-1. Even if the cell junction were oriented correctly to allow current to flow, the 1-10 Ohm-cm internal wafer resistivity of PV silicon may still be too high to drive a suitable plating current. Additionally, wafer resistivity variations along the ingot and processing conditions will lead to different solar cell internal resistances which would widely affect plating parameters across samples. Alternatively, electrical contact on the front is more technically challenging to implement but would omit the internal resistances of the solar cell from the electrochemical circuit.

The goal is to plate to a wide area on the front of the solar cell in the shape of a front grid, so electrical contact should be made close to the edges of the cell to avoid interference with the plating area. Since the top layer of ITO for SHJ cells or silicon for TOPCon are poor conductors across the large cell areas, a conductive seed layer is necessary to maximize current distribution across the wafer as shown in Fig. 2-2 and minimize current crowding near the electrical contacts.

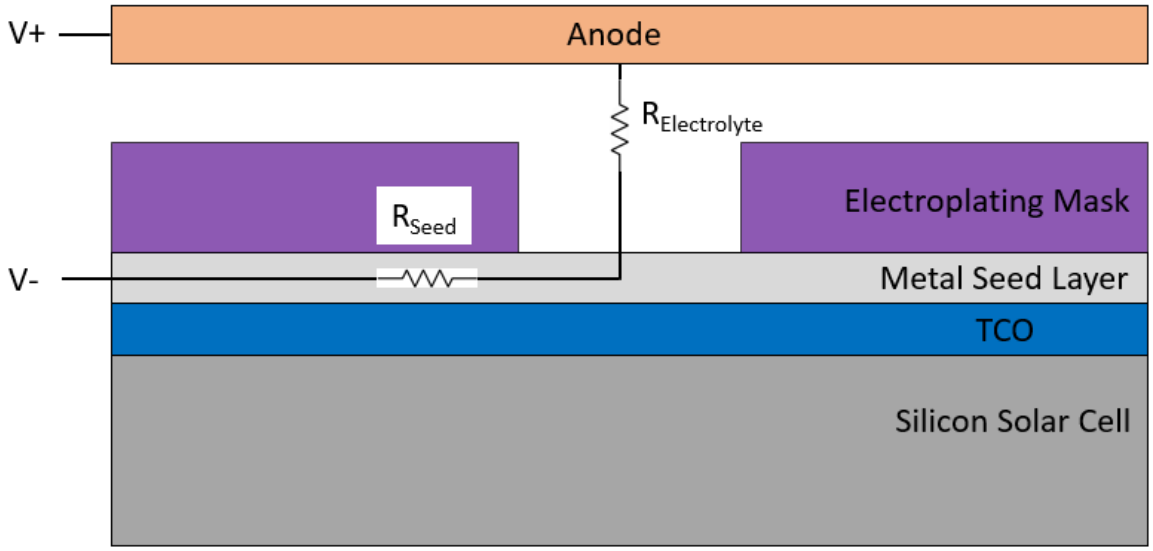

Fig. 2-2. Diagram showing the alternative front contact method for SHJ solar cells. The seed layer is electrically contacted from the edges of the wafer in multiple locations to maximize current uniformity across the seed layer. Contacting the seed layer makes for a more difficult physical setup, but the internal equivalent circuit of the solar cell is circumvented. As with Fig. 2-1, the $R_{Electrolyte}$ includes all bath and electrode capacitances and resistances.

2.1 LIGHT INDUCED PLATING (LIP)

LIP is a solar cell front metallization technique first introduced as a patent by Späth in 1973 [58] and reviewed by Mette [59]. This plating technique utilizes bright lights to generate excess electrons on the surface of the solar cell to provide activated sites for positive metal ions in the plating electrolyte. Fig. 2-3 describes the LIP process. For this process to work, the n-doped region must be on the front of the solar cell. LEDs are present in the plating bath and shine onto the front surface of the solar cell. A metal brush contact is placed on the rear of the solar cell at ground potential. This method of plating is technically known as bias assisted LIP, but since it is the only LIP method used in this work, will be referred to only as LIP. The incident light on the solar cell from the LEDs generates electron-hole pairs in the emitter. Positively charged holes in the emitter are

drawn to the ground electrode on the rear of the cell while negatively charged electrons diffuse to the surface. An excess carrier concentration of electrons at the surface of the emitter gives the surface a negative charge. A mask whether dielectric or photolithographic is present on the emitter that defines the front grid pattern. Positively charged metal ions in the bath are drawn to the entire emitter but can only bond where the electrons are exposed on the surface of the silicon, and not where the insulating mask is present. The metal ions near the exposed regions of the emitter are reduced and form a solid metal on the emitter.

When performing LIP on DJ solar cells, the front grid would normally be deposited directly onto bare silicon once the dielectric mask is exposed. Thus, an intermediate buffer is usually plated first to prevent diffusion of plated copper into the silicon bulk. Thus, a thin ~1um LIP nickel (Ni) layer is first deposited on the silicon surface, since Ni silicides have been shown to act as a diffusion barrier to copper [60], [61], [62]. After the nickel is deposited, copper plating can then commence onto the nickel layer. LIP is not used to create copper front grids in this work, but LIP nickel is one of the seed layers tested in this work for SHJ solar cells.

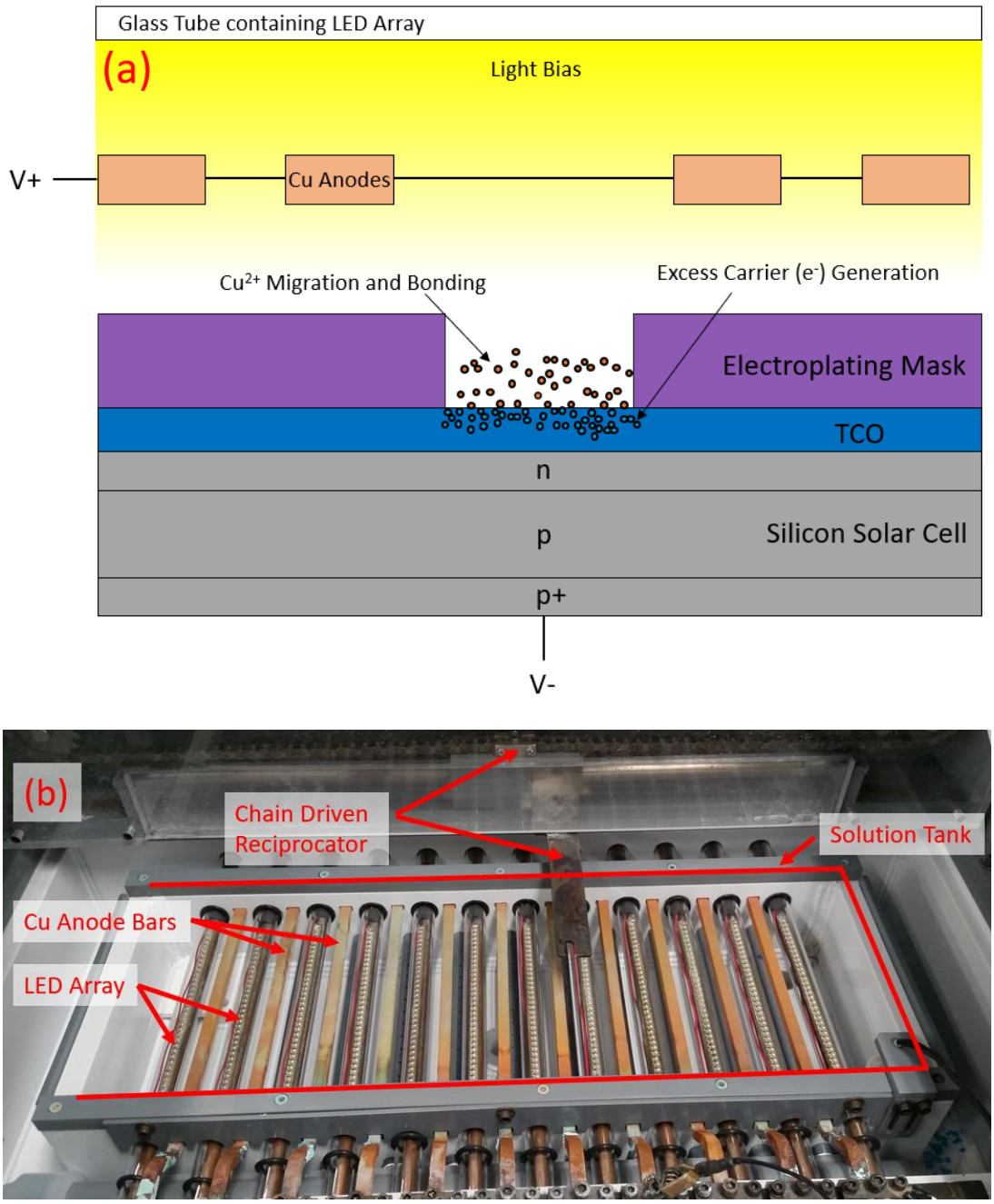

Fig. 2-3. (a) Diagram of LIP Cu plating and (b) custom created equipment by Technic Inc. (a) Positive potential on the submerged Cu anodes provides a corrosion source and a potential bias to increase plating rate due to the solar cell operating near short circuit conditions. Light bias on the solar cell splits the quasi-Fermi levels on the solar cell and creates a large excess of electrons on the surface which provides activation sites for the Cu to bond. Electroplating mask can be photoresist, or an ablation patterned dielectric film. In (b), a wafer was place in a custom plating holder and would be moved (reciprocated) left and right over the anodes to provide uniform plating.

2.2 SHJ SOLAR CELL FABRICATION

Unless noted otherwise, Cu-plated SHJ solar cells were made on 120-μm-thick n-type CZ wafers with 3-4 Ω-cm resistivity. The wafers were textured in KOH and cleaned using RCA-B, Piranha and BOE, to remove metal, organic and surface oxides respectively. Deposition of intrinsic α-Si followed by doped α-Si occurred on both sides of the wafer. The front received p-type α-Si and the rear received n-type α-Si. In this work, two types of TCO were used on the front of the cell: 1) ITO with a high free carrier density (n_e) and 50 Ω/□ sheet resistance (R_{sheet}) and 2) ITO/SiOx stack with 100 Ω/□ R_{sheet}. ITO/Ag was sputtered at the back side of the solar cell to form a rear contact. Next, a variety of seed layers: silver (Ag), nickel (Ni), chromium (Cr), and titanium (Ti), approximately 100 nm thick, were either sputtered, evaporated, or plated on the front side of the solar cells. Two separate Ni seed layers are utilized and are distinguished by the deposition method. A vacuum sputtered physical vapor deposition (PVD) Ni layer and an LIP deposited Ni were tested and referred to as PVD Ni and LIP Ni respectively. The fronts of the cells were covered in a photoresist mask to define the front grid pattern on the solar cell. The resist mask was formed on the front side of the cell using three different methods: commercially available screen-printed photoresist, industrial dry film photoresist and spin-on photoresist. For the LIP seed layer, only the dry film photoresist was used, and it was rolled directly on the ITO without a seed layer. The process flows are shown in Fig. 2-4. Once the masks were in place, the wafers underwent contact electroplating to plate the fingers and busbars on the front of the solar cell. Plating was followed by a photoresist etch in a heated, dilute sodium hydroxide bath. For most of the seed layers, excluding the LIP nickel, the seed metals needed to be deposited prior to the photolithography step. This means the entire

front of the wafer is coated with the seed metal which needs to be etched. Etchants for Ag, Ni, Cr and Ti were individually composed and used to clear the surface of any remaining seed metal. What remains is the blanket ITO on the surface with the plated copper front grid.

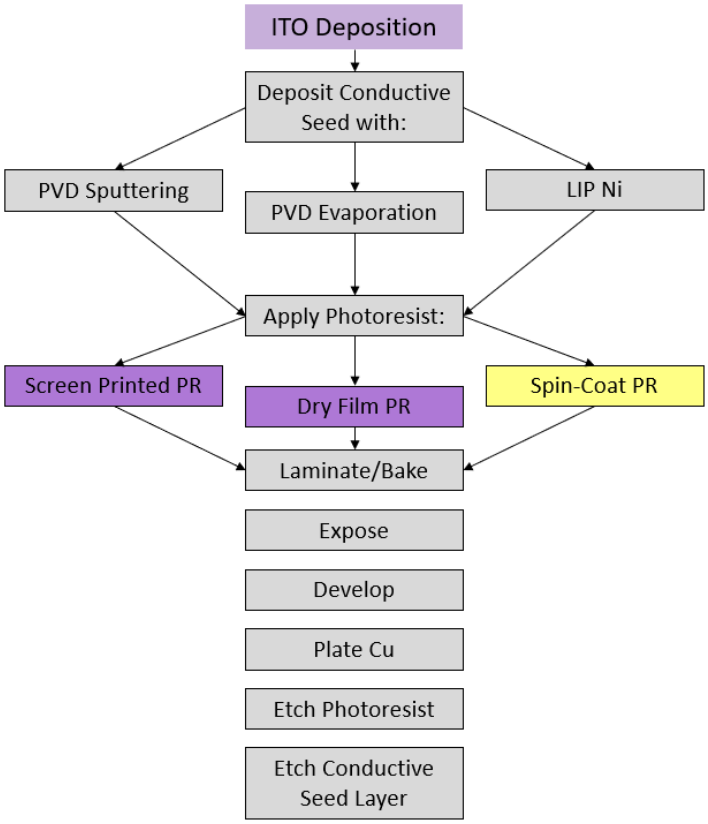

Fig. 2-4. General process flow for the SHJ seed layer and photolithography applications as well as removal.

2.2.1 Seed Layer Processing

The Ag and PVD Ni seed layers were deposited via vacuum sputtering, the chromium and titanium were deposited via evaporation, and the LIP Ni layer was deposited using LIP. Since the ITO could only be processed in the vacuum sputtering tool, the only seed layers that could be deposited without breaking vacuum were Ag and PVD Ni. Thus, the

ITO was exposed to ambient air prior to depositing PVD Cr, Ti, and LIP Ni. After photolithography, the wafers were plated with copper. In the case of LIP Ni, the native oxide which forms provided such poor adhesion to the plated Cu that the Cu portion of the front grid simply fell off after plating. No such issue occurred with the other seed layers, so the LIP Ni seed layer cells were placed in a dilute etchant immediately prior to immersion in the electrolyte bath for plating, the goal of the Ni etchant being the removal of the native Ni oxide layer.

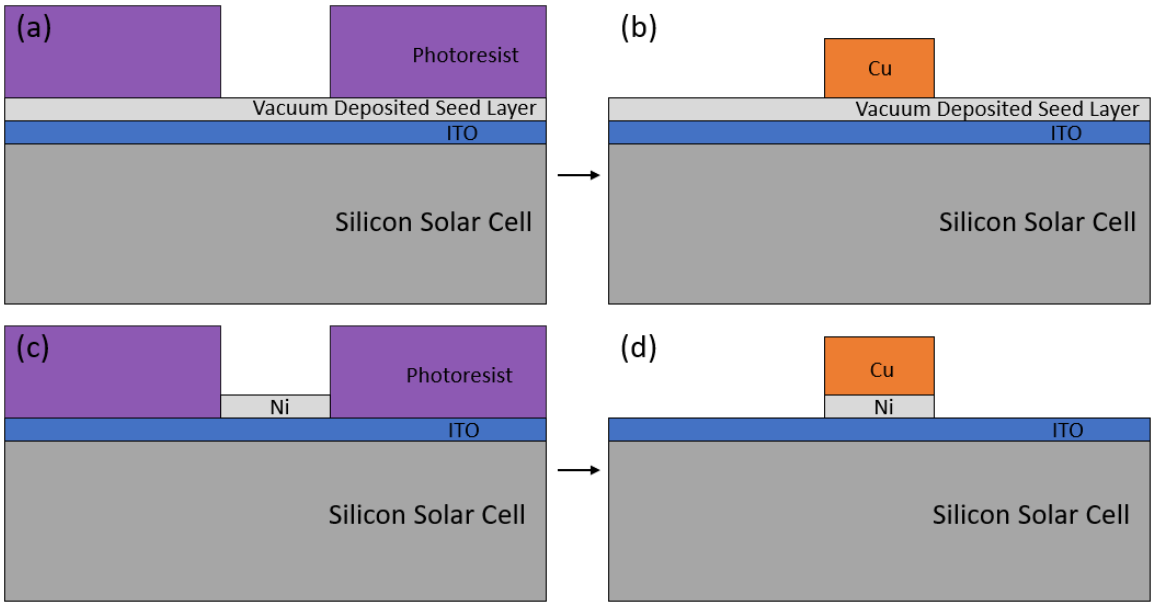

Fig. 2-5. Summarized processing steps for each seed layer type. (a), (b) Seed layers deposited in vacuum, e.g., sputtering and evaporation, such as Cr, Ti, Ag, and PVD Ni, needed to be deposited prior to photolithography due to the organic nature of photoresist. (c), (d) The LIP Ni seed layer was deposited in electrolyte at room temperature, so the seed layer did not need to be etched away after photolithography.

2.2.2 Photolithography

Each of the three negative photoresist types used in this work conformed to the same basic steps of photolithography used in the IC industry shown in Fig. 2-6. A negative resist type was chosen due to the lower cost and different varieties, among other advantages, for

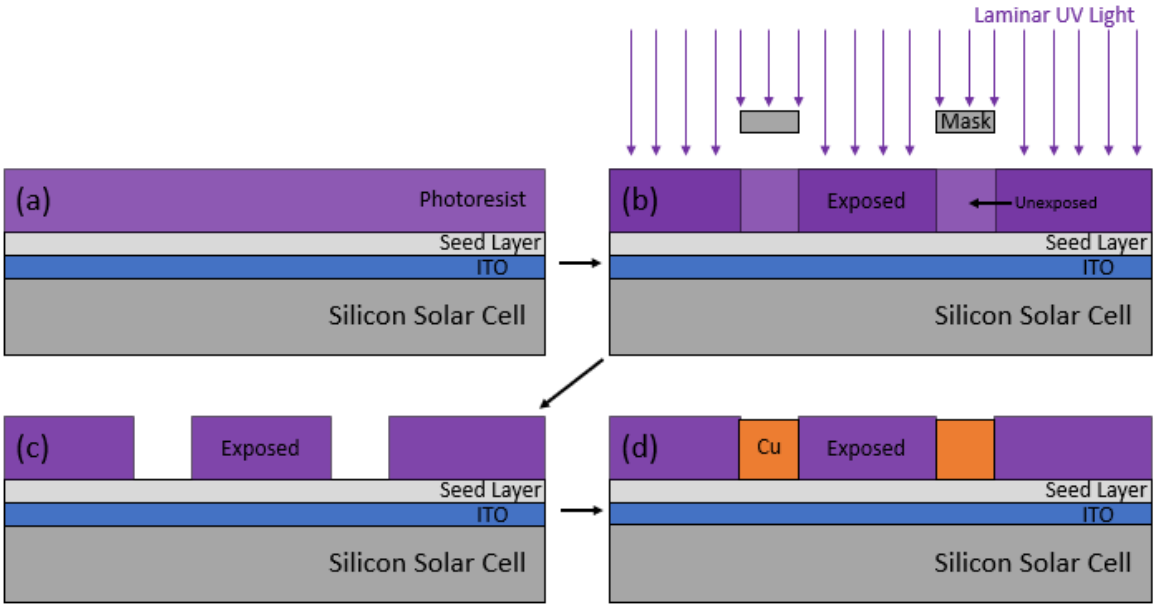

Fig. 2-6. General photolithographic processing with all three negative photoresists. (a) Photoresist is deposited and cured, followed by (b) UV exposure with a mask of the front grid design, (c) developing the unexposed photoresist, and finally (d) plating in the developed regions.

this work [63]. Despite the resolution typically being poorer for negative compared to positive resist, the smallest desired feature size of 40μm for finger widths far exceeds the limitations of industrial negative photoresists. The resist was deposited in a manner depending on the type of resist used e.g., spin-on, screen-printed or laminated and the actual cells are seen in Fig. 2-7(a), (b), and (c) respectively with measured profiles. Liquid spin-on resist was applied via a spin coater and cured on a hot plate. Sheets the size of the wafer were cut from the solid dry film photoresist roll and applied to both sides of the wafer. The wafer and cut photoresist were covered on both sides with silicone sheets and cured in a vacuum laminator system used for solar cell module fabrication. The laminator pressed the photoresist onto the solar cell to heat each side and the vacuum removed air trapped under the photoresist. The screen-printed photoresist composed a thick paste and was applied in the same method as an Ag screen-printed front grid. A squeegee passed over

a screen mesh and squeezed the photoresist emulsion onto the wafer, which was later cured in a muffle furnace. The mask used for the screen-printed photoresist was completely open, so photoresist was placed over the entire cell. A mask covering the front grid pattern was attempted, but the screen-printed photoresist used was not viscous enough to achieve maintain the front grid pattern i.e., paste seeped under the mask into the channels.

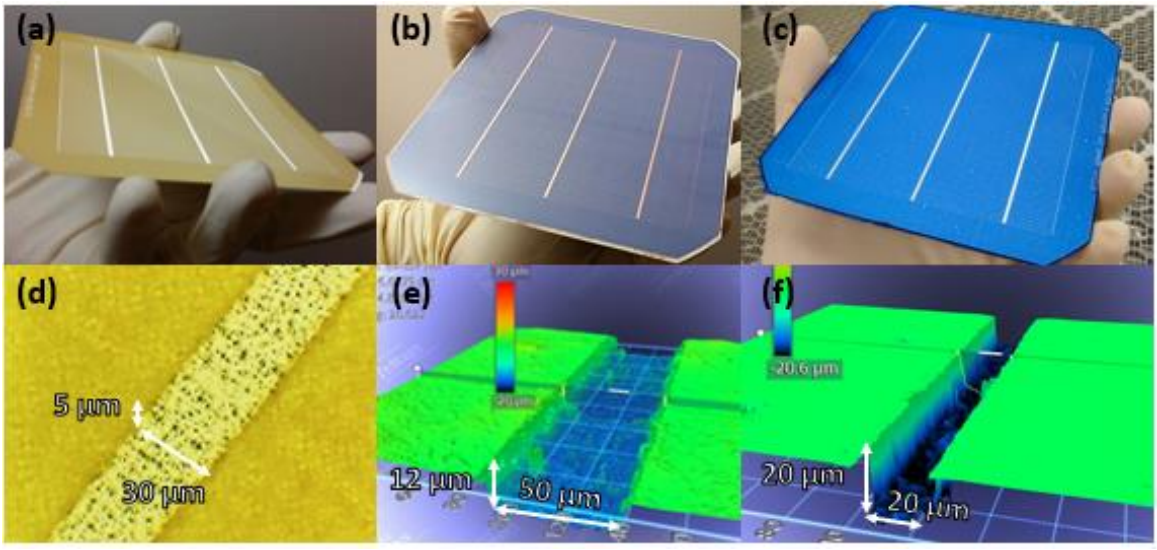

Fig. 2-7. Pictures showing the three photolithography methods used in this work to pattern the front grid. Images of the (a) spin-on resist, (b) screen-printed photoresist, and (c) the roll-on dry film photoresist. The corresponding (d) optical microscope image of spin-on resist, and optical profilometry images of (e) screen-printed and (f) dry film resist exposed finger profiles below.

After deposition, the screen-printed and spin-coated resists were cured to solidify and bond to the solar cell and although the dry-film was not liquid, it still required the curing step to bond to the solar cell. Once cured, a UV mask in the shape of the front grid was placed over the solar cell and the photoresist was exposed in a UV exposure tool. Each photoresist underwent development in their respective chemical developer bath, to remove the non-exposed resist and reveal the front grid pattern for plating (see Fig. 2-7(a)-(c)).

Each photoresist was iteratively tested through available photolithography equipment to produce the finest resolution and optimal exposed front grid. Each photoresist had different resolution due to the composition, so the produced finger widths and heights, as well as individual photoresist capabilities are reported in Table 2-1. In addition to the resolution, quality of each resist was also examined in this work since each photoresist is targeted for different markets and price points. AZ spin-on photoresist used in this work could achieve the highest resolution, while the screen-printed resist displayed the poorest resolution. The heights of the spin-coated photoresist and the screen-printed photoresist could be altered depending on spin speed and screen mesh and gap parameters respectively, but the spin-coated photoresist was limited to 10 μm for this work, and the screen-printed photoresist could not exceed 15 μm due to the rheological properties of the photoresist. Printing, curing, and then printing a second layer of photoresist was attempted similar to the methods performed for double screen-printed Ag front grids [64], but exposure became difficult due to the thickness causing unopened lines or largely overexposed regions. Finally, a special dry film photoresist, which could achieve 20μm resolution while having 20-30μm thicknesses, was used.

Table 2-1. Measured physical characteristics of each photolithography method used in this work.

Photoresist	Resolution	Full Size[1] Resolution	Height (um)	Relative Cost	Throughput Description
Screen-Printed	45µm	60-70µm	10-15	$	Seamless integration with current screen-printer technology
Dry Film	20µm	40µm	20	$$[2]	Mass Production Ready[3]
Spin Coated	10µm	30µm	5-10	$$$	Research tool – very low throughput

[1]Full size cell resolution is considered consistent coverage with no finger breaks in a 10cm x 10cm cell
[2]Cost is considered at current state and not in mass production setting. With scale, costs decrease.
[3]Dry film photoresist is sold on large rolls meant for existing PCB production lines, so integration for solar would be a technical and not resource task.

2.2.3 Experimental Setup of Contact Electroplating for SHJ Solar Cells

The contact electroplating was performed by making electrical contact to each end of the busbars on the cell for a total of 6 contacted points as in Fig. 2-8. In some experiments, metal oxides were stripped using their respective wet etchants immediately prior to Cu plating. Similarly, prior to electroplating the LIP Ni, the ITO surface was prepared using a dilute ITO etchant. All cells were capped with a contact electroplated, 200 nm layer of tin (Sn) for soldering. After electroplating, photoresist masks were stripped, and seed layers were etched. Finally, the cells were annealed at 200°C for 30 min in a muffle furnace. For ITO/SiO_x stacks the cells were finished by the deposition of the SiO_x layer above the electroplated metallization.

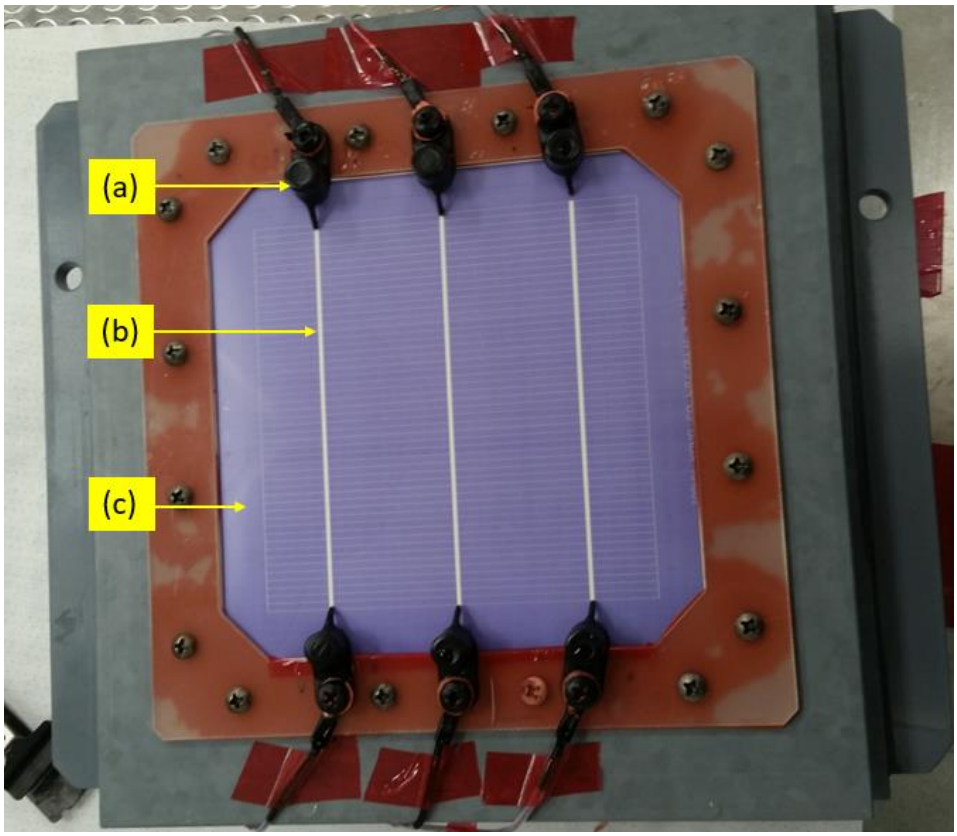

Fig. 2-8. Custom contact electroplating apparatus made for solar cells with a solar cell harnessed in. Highlighted are the (a) ground probes to charge the metal seed layers on the front of the solar cell to complete the electrochemical circuit, (b) busbar and finger front grid pattern exposed in the photoresist, and (c) face of solar cell with purple screen-printed photoresist.

2.3 MEASURED RESULTS OF SHJ CELLS

Characteristic measurements for the electroplated samples were performed using the following equipment: IV curves were measured using an FCT-400 tester from Sinton Instruments, specific contact resistivity was measured using the transfer length method (TLM) on dedicated wafers with TLM test structures, electroluminescence (EL) and photoluminescence (PL) images were captured using an in-house tool with a camera and appropriate IR and visible light filter, line resistance was measured using a four-point probe, and adhesion was measured using a 180 degree pull test on an Instron.

2.3.1 Front Grid Optimization

Prior to measuring the final results of a solar cell, there are many factors to consider when applying a front grid pattern. The novel level of control and application of electroplated Cu to SHJ cells in this work requires a grid parameter optimization so that gains made with electroplated Cu on the front grid are not concealed in offsets by poor grid modifications. For example, when the metal used for the front grid is screen-printed Ag, maximum heights are limited by the screen-printer and paste properties, so maximum finger widths are thus also limited. When electroplating a more conductive front grid such as Cu, heights are limited to each individual photolithography process, as well as resolution, so finger spacing needs to be optimized for each process. To better understand the tradeoffs involved when optimizing the electroplated Cu front grid in SHJ cells, an analytical model was built to provide reference data. For simplicity, a 3BB solar cell is consistently used across all photolithography methods since soldered ribbons and stringing are beyond the scope of this work. The model considered a standard industrial SHJ cell with 80-μm-wide screen-printed fingers as a baseline. The results of modeling suggest that replacing Ag fingers with Cu fingers of the same width can reduce line resistance two times and overall series resistance of the solar cell by 0.3 Ω-cm^2 leading to 0.4% absolute efficiency increase. If Cu fingers can be made 30-μm-wide, both series resistance and front grid shading can be reduced leading to 1% absolute efficiency increase. Finally, if an ITO/SiO_x double layer antireflection coating is used, the generation current of the cell will be increased by 1 mA/cm^2 giving a total 1.5% absolute efficiency increase. This structure is allowed because the 30-μm-wide fingers can be spaced closer, so that the cell can tolerate the higher sheet resistance of the ITO/SiO_x stack. Bulk and front optical improvements

would of course increase efficiency, but this work only examined the Cu metallization compatibility with the existing SHJ structure, and the closer spaced fingers that thinner, higher conductive fingers would allow on the front of the SHJ solar cell. Overall, the model expects 1-1.5% efficiency gain by switching from printed Ag to plated Cu. In the model several assumptions were made, which imply the requirements to copper metallization. These are idealities to be used as a "best case scenario" to achieve the 1.5% efficiency increase and are noted in the corresponding data plots in Section 2. These modelled values include: an electrical contact to the metal seed layer and ITO with < 0.5 mΩ-cm2 specific contact resistivity and a tall enough finger height to produce < 0.5 Ω/cm line resistance. Physical adhesion has little to do with cell electrical results but is still an important metric for industrial applications. Thus, passing a tape test and/or achieving >1N/mm pull strength of a soldered busbar was considered an acceptable adhesion result for this work.

2.3.2 Electroplated Fingers and Electroluminescence (EL)

The quality of the plated fingers in this work was examined by a mixture of visual inspection and electroluminescence (EL). EL is an important tool for qualifying front grid series resistance of the solar cell. The concept of EL is to externally bias the solar cell, so the cell functions in reverse. By applying a current to the busbars of the solar cell, electron hole pairs are electrically generated near the electrical contacts and the cell emits light. The solar cell is rear contacted on a conductive chuck so current flows in through the top of the cell and out of the bottom. The bias current during EL is very large and so a great excess of electron-hole pairs are generated near the contacts. Some make it to the contacts, but most recombine and emit a photon. Fig. 2-9 demonstrates the EL process.

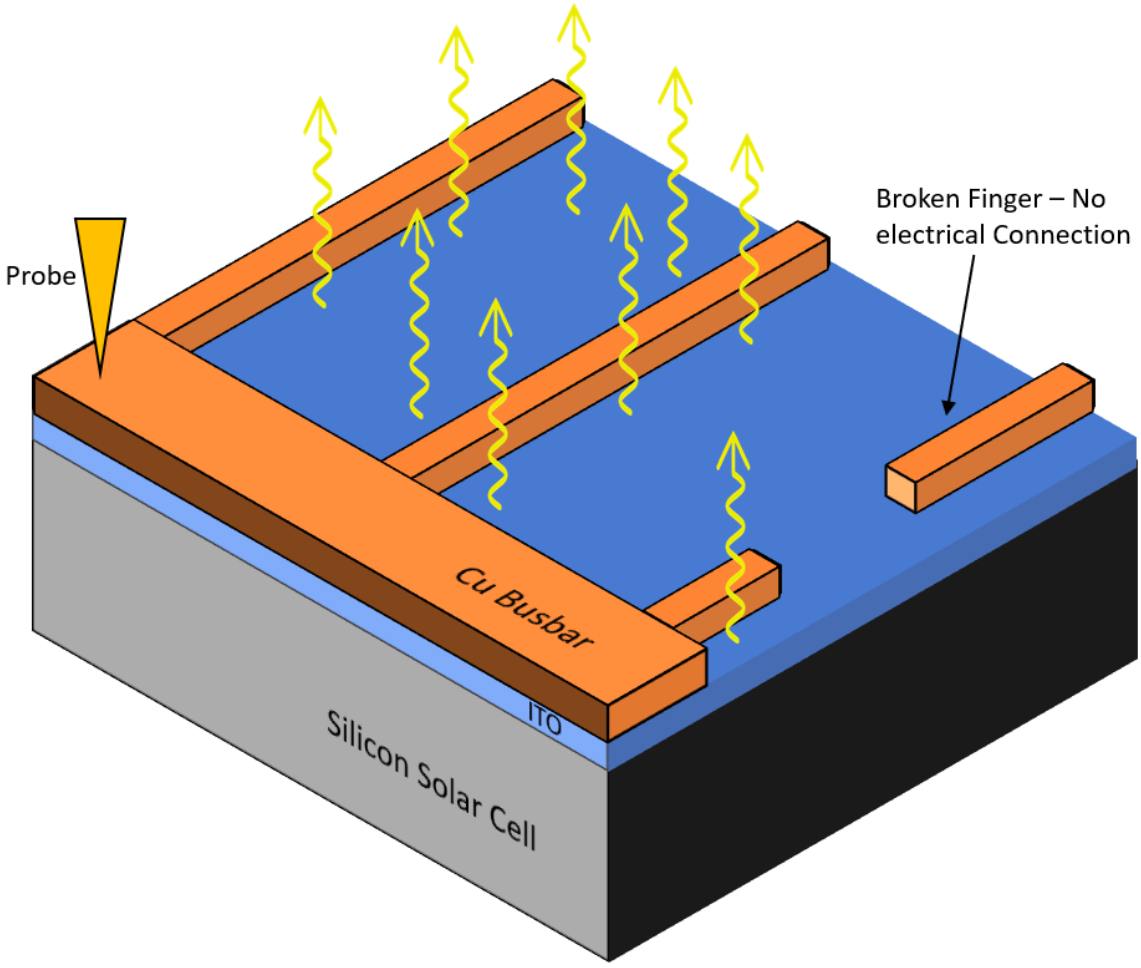

Fig. 2-9. Diagram showing the process of electroluminescence. Photons are generated anywhere close to the current source. Relative light intensity is used as a tool to determine if the current is not reaching the cell i.e., there are areas of high electrical resistance. Also shown is a broken finger due to some processing error, which would show up as a black spot in EL, since there is no way for the current to reach the broken end from the current source, labelled probe in this figure.

Due to the internal resistance of solar cells, areas on the front of the solar cell that are far away from a contact point appear darker, since fewer electron-hole pairs are generated due to potential losses away from the contacts, as shown in Fig. 2-10(a), (b). Similarly, broken fingers can be spotted in Fig. 2-10(c) where they begin with normal EL intensity near the busbar and drop off in a single step at some point along the finger. A finger that is broken

either receives no electrical connection or is contacted by a busbar that is farther away resulting in shading.

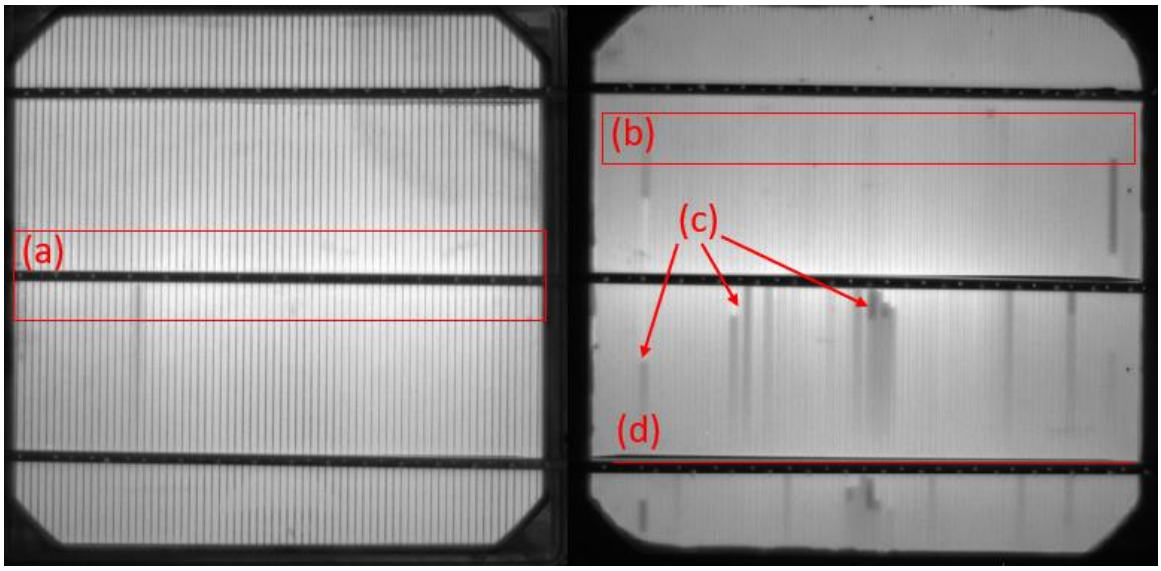

Fig. 2-10. EL images of two solar cells with different front grid integrities. The right solar cell has a (c) large number of broken fingers and a more resistive front grid. Areas of note are (a) regions of high brightness near the busbars where most of the current flows and (b) areas of much lower brightness where resistance of the cell contributes to current losses that generate less electron-hole pairs that recombine and generate photons. Also noted are the (c) shaded regions that are reminiscent of broken fingers and (d) the busbars that are electrically connected to the EL power supply.

There is a trade-off for finger width between increasing conductivity of the front grid and decreasing incident light absorption area for the solar cell. Increasing the conductivity by increasing finger width reduces the series resistance but decreases the total current of the solar cell due to increased shading since the front grid is opaque. Conductivity of the fingers remaining constant, optimal power gains can be realized with thinner fingers and smaller spacing between the fingers. However, due to the many novel parameters tested here e.g., seed layer compatibility, photoresist quality, etc., this optimal point was not reached. For example, while a photolithography process may allow for 10μm wide fingers

with 100μm spacing, the different contact resistances of the seed layers introduce a third variable of optimization that may become too high with 10μm fingers. Since the goal of this study was to compare the compatibilities of each method with SHJ solar cells, 40μm was set at an arbitrary limit for the thinnest fingers, and further optimizations for efficiency did not take place.

Before front grid fabrication occurred, each photoresist was tested using in-house photolithography equipment. One of the main issues that arose with photolithography was finger non-uniformity and breakage, or when one or more parts of a front grid finger are not physically or electrically connected to a busbar. Such fingers on the front surface contribute to cell shading, but do not contribute to current extraction. While all photoresists had a 40um feature limit or better, the screen-printed resist was found to be more susceptible to partially or fully exposed finger regions, leading to less uniform fingers and breakages. For all photoresists, this is caused by over or underexposure of fingers, due to a non-optimized time in the UV exposure tool and/or chemical developer. These times were critical to create uniform finger openings when the fingers approached the resolution limits of the photoresist. As an example, the dry film photoresist could easily achieve 20um finger channels as shown in Fig. 2-7(f), but broken fingers became more prevalent as the limits of the resists were reached, so it was safer to increase the finger width to reduce losses in the front grid.

The breakages were easily visualized with EL. Disconnects caused by finger breakages were shown in EL as dark channels that run parallel to the fingers. Similarly, highly resistive fingers that may be too narrow for the optimized finger spacing will show a decrease in the brightness as the finger moves away from the busbar, i.e. photolithography

finger slots that are overdeveloped or underexposed lead to narrower channels for plating fingers. Fig. 2-11 shows a plated copper finger with the screen-printed photoresist still present on the solar cell. It can be clearly seen that photoresist is jutting from the sidewalls on the scale of 10um into channel space meant for the growth of copper. This leads to varying, and in the case of the cell in Fig. 2-11, larger resistance along length of the finger.

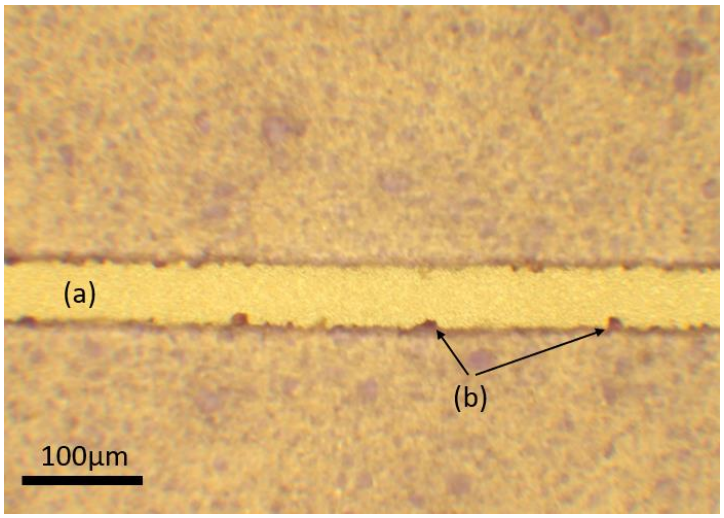

Fig. 2-11. Optical microscope image of (a) a plated copper finger on an SHJ solar cell with screen-printed photoresist. The photoresist is still present on the cell outside of the finger. The screen-printed photoresist was more susceptible to problems such as (b) overexposure of certain regions leading to inconsistent finger cross section. Not shown is possible resist stuck under the electroplated copper due to difficulties in removing all photoresist during development.

What is not shown in Fig. 2-11 is the possibility of photoresist particles left in the finger channels, a clear indication of underdevelopment. This can also lead to finger breakages, or more likely increased contact resistance between the copper, the trapped photoresist particle, and the front of the solar cell. This forces electron hole pairs near the photoresist particulate to travel farther to get to the finger. While no picture was captured of this phenomenon, it did occur and was seen under the optical microscope and appeared in EL as a dim region near the particulate.

When photoresist recipes and front grid structures are optimized to achieve desired finger widths with no breakages, the actual plating event could still lead to finger breakage. The issue lies with the composition of the photoresist and the width of the channels formed for the fingers. The photoresist is extremely hydrophobic and the surface tension of water, which composes most of the plating solution, is very high. Dry solar cells with photoresist, when placed into plating solution, have a difficult time removing the oxygen between the channel walls of the photoresist. Even with pumps, which cycle solution in the bath by spraying solution onto the face of the solar cell, oxygen isn't always removed from the channels of the fingers. Trapped oxygen in the channels prevent plating solution from entering the channels, which then prevents plating from occurring in the affected area. This can be observed in Fig. 2-12, where a bubble was present in the photoresist channel walls, leading to a broken finger. Evidence of the bubble quickly disappears after the metal seed layer is stripped, since the metal etchants for the seed layers typically also etched copper. Thus, this effect needed to be observed after stripping the resist but before etching off the seed layer. The bubble problem ended up being resolved by pre-wetting the silicon wafer prior to entry into the plating bath. A high-volume deionized water sprayer could wet the surface of the entire exposed front grid, even with the thinnest finger channels tested. By pre-wetting the channels, electroplating solution was able to wick to the already wetted surface and flow through the channels. Once this method was initiated, no further finger breaks were measured from EL or observation, supporting the hypothesis that trapped oxygen was leading to incompletely plated fingers during the plating event.

One other issue observed in this work was a phenomenon coined "mushrooming" of fingers. When a metallization process arises such as electroplating where one can guarantee

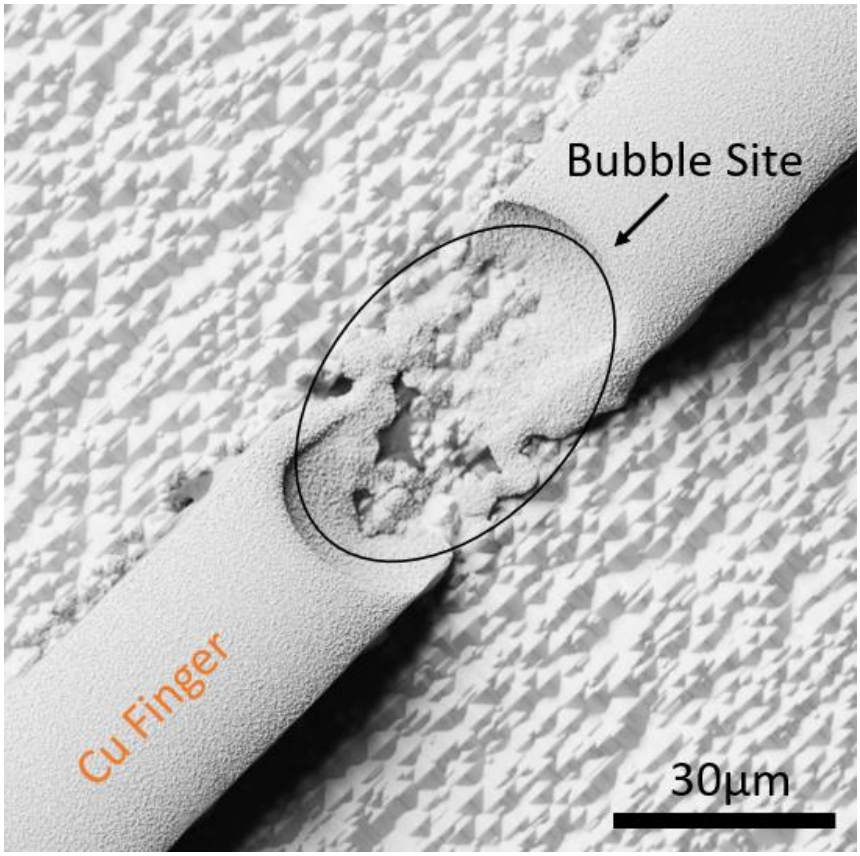

Fig. 2-12. SEM image of a broken copper finger after stripping of photoresist. The conductive seed layer was left on for the image. The smooth round profiles constantly found on the edges of all bubble sites on the finger support the hypothesis that a bubble was present. Contrast this with a random edge pattern from an over-exposed region on the finger.

lower front grid resistance by leaving the power supply on in the plating bath to increase the finger height, it is tempting to do so. However, once the plated regions of the front grid exceed the height of the photoresist, this mushrooming can be observed. Since the walls of the photoresist confine the plating to between the channels of the fingers and busbars, the surface area to be plated remains approximately constant for the duration of the plating event. Once the height exceeds the photoresist thickness, plating occurs simultaneously from all directions, meaning the finger will grow outwards in all directions, instead of just vertically. This can be visualized in Fig. 2-13 by looking at the cross section of a

mushroomed finger and the issues can be seen when viewed from an angle as in Fig. 2-13(b). Two events occur as a result of electroplating beyond the mask height: 1) the larger

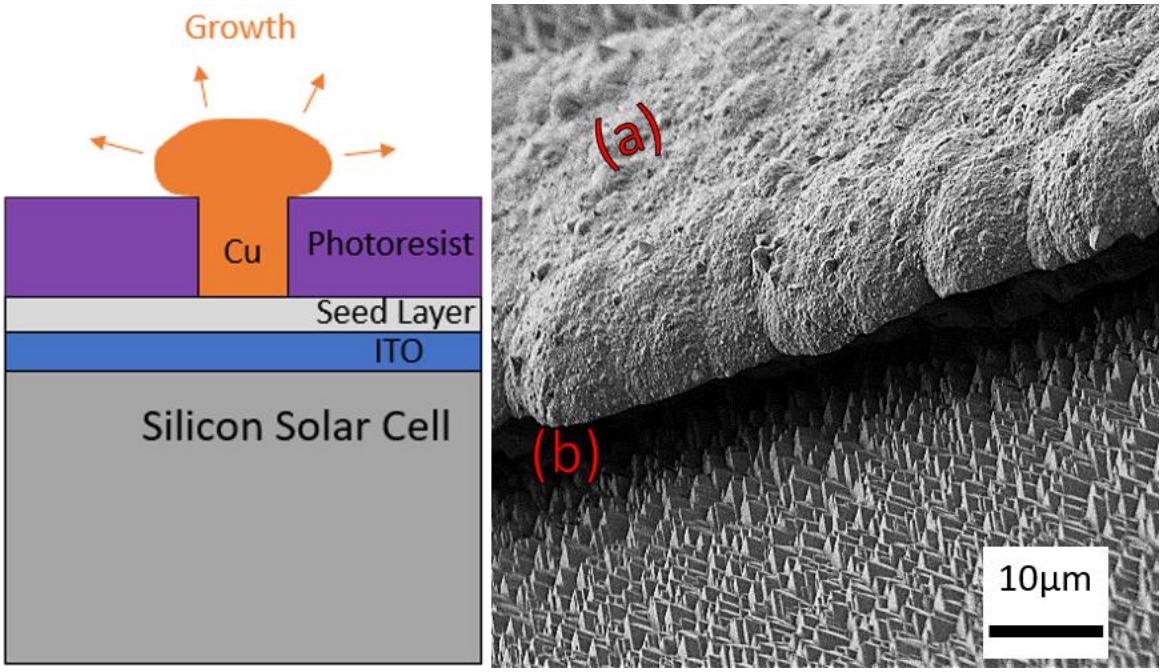

Fig. 2-13. Visualization of Cu mushrooming effect. Cross section diagram explains (a) Cu growth over the photoresist and a diagonal view SEM image of the effect. The (b) shadow in the SEM image shows the Cu extension shading the silicon surface.

exposed surface area of the top of the mushroomed finger will lead to faster plating rates, which further exacerbate the problem and 2) the optical width of the finger will increase. Mushroomed fingers begin to shade more solar cell surface which reduces the current and lowers efficiency, offsetting the gains made from plating more and reducing finger resistance.

The final finger profiles for using photolithography varied with the photolithographic material used and can be observed in Fig. 2-14. The spin-on photoresist could reliably achieve 30um wide finger profiles with an optimized finger spacing, but the thickness of the photoresist was limited to 5um tall. The screen-printed and dry film resists were limited

to 60um and 40um finger widths respectively due to the higher prevalence of photolithography induced finger breakages thinner than this value. However, the thicknesses of the screen-printed and dry film resists were notably higher than that of the spin-on resist, 12um and 20um respectively. This allowed for taller profiles, reducing resistance of the fingers. The spin-on and dry film resist were of integrated circuit quality and were much easier to optimize given the tools used in this work to expose and cure the resists. The SEM images in Fig. 2-14(d), (f) show that despite the finger size limitations, the copper plated fingers were extremely uniform along the length of the fingers. Conversely, Fig. 2-14(e) shows that the resulting plated finger uniformity was much lower for the larger screen-printed finger. This was expected given the consistently poor removal of screen-printed photoresist during development and characterized in Fig. 2-11.

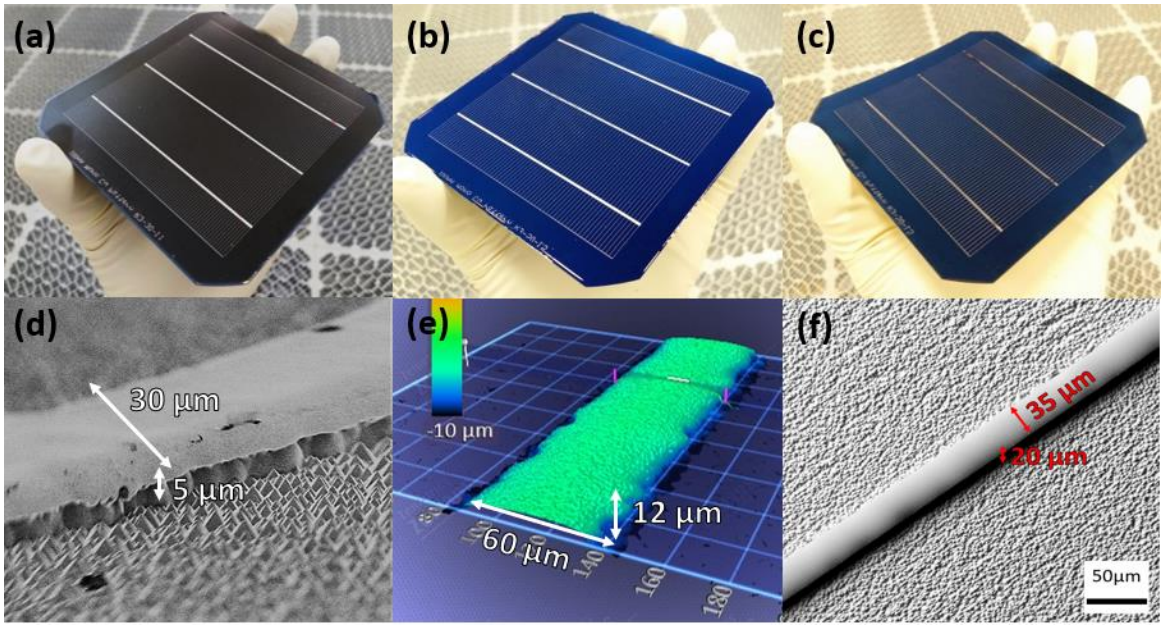

Fig. 2-14. (a)–(c) The photos of the resulting plated profiles of cells patterned by spin-on, screen printed and dry film photoresist respectively. (d)-(f) SEM and optical profilometry of a finger from (a)-(c) respectively.

2.3.3 Plated Copper Adhesion

Adhesion is an important metric for industry to determine front grid and wafer processing reliability, but unfortunately is an obscure area of research for solar. Contrary to electrical and material parameters for solar, which are empirically and theoretically well-known, there is no consensus to what sufficient physical adhesion for a solar cell front grid is [65]. Thus, this work defined and distinguished three levels of adhesion that could be relevant to the solar industry. The first level was when the cell could be successfully probed as seen in Fig. 2-15a, after all processing was finished. This test is important because failure would mean the cell is making weak physical and electrical contact with the front grid. This extends to processing as well, as a front grid that couldn't be probed would also become dislodged during the many stressful processing steps following metallization including thermal stresses in soldering and lamination, and the physical stresses of handling. Thus, probing the front grid implies the cell could survive some form of production. The second level of adhesion was when the cell passed a tape test, which was done using a 401 film, similar to scotch tape. This is the first real test of the front grid adhesion, as it places a large stress on the very small fingers. As seen in Fig. 2-15b, a solar cell is placed on a vacuum chuck so that there is a uniform holding force on the back of the cell. A piece of tape wider than the busbar is applied along the busbar and the tape is pulled at a 90-degree angle or normal to the solar cell surface for the entire strip of tape. The tape may or may not rip the busbar and/or fingers off the cell or each other determining the pass or fail of the tape test respectively. This more vigorous test provides a more complete picture on how a cell could survive the remaining production steps and possible longevity in a module. In addition to the solar cell stresses listed previously, solar cells tend to be

stacked and consistently rub against other cells in production. Stacking is useful for pick and place machines for modules or soldering stages and the stresses imposed from cell friction during stacking can be simulated this way, with a forceful pulling of the front grid using the tape. The third and final level of adhesion was when the cell passed a 180 degree pull test with a soldered ribbon with more than1 N/mm pull strength, using an Instron [66]. 1N/mm was arbitrarily chosen considering 2.5 N/mm is the force required for silicon wafer

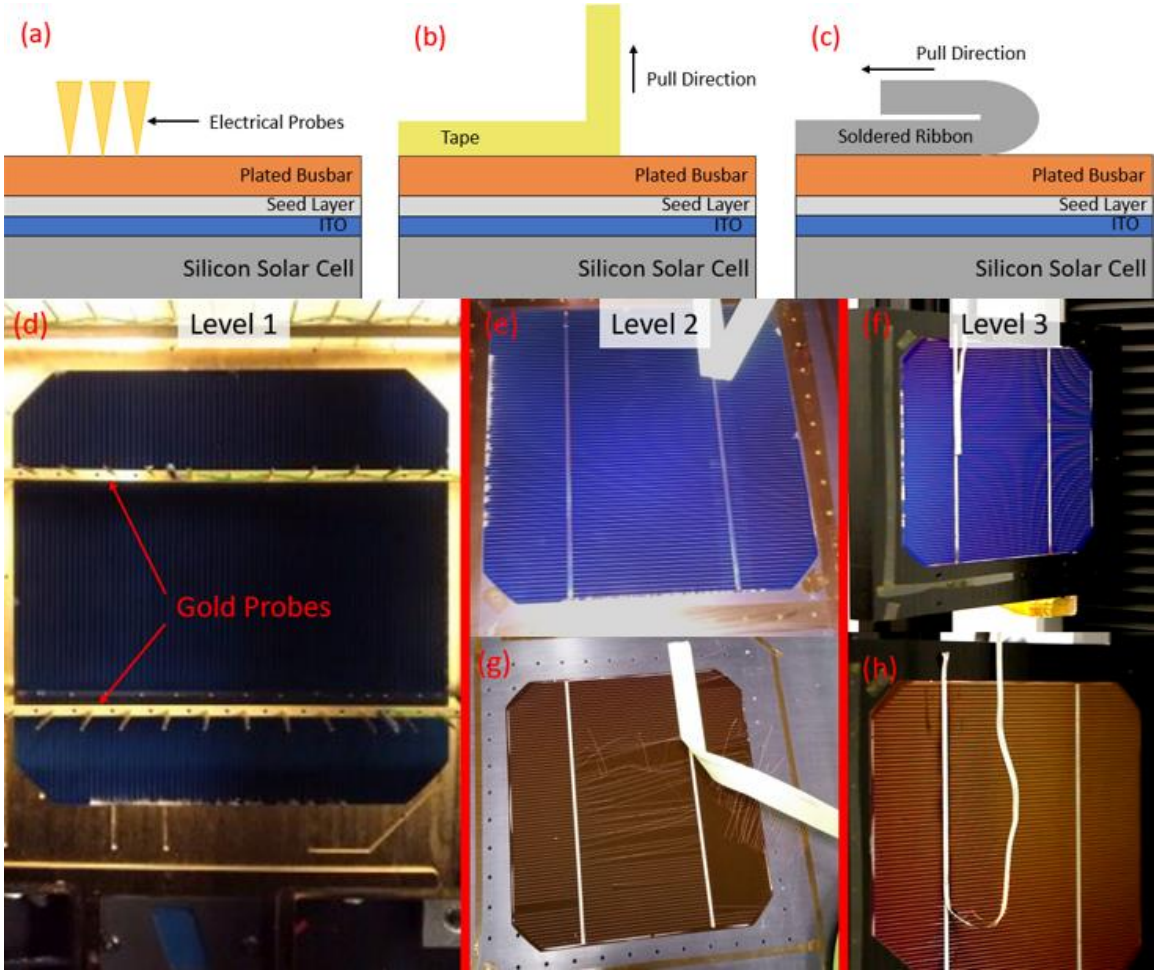

Fig. 2-15. (a)-(c) Description of 3 levels of adhesion followed by (d)-(h) passing and failing of subsequent tests. (a) The first level of adhesion was probing the sample and is shown successfully in (d). (b) The second level of adhesion is the 90-degree tape test on a vacuum chuck with a wafer that (e) passed and (g) failed. The final level of adhesion was the measured Instron 180-degree pull test with a soldered ribbon and wafers that (f) passed and (h) failed.

breakage [67]. If a front grid passes the first two levels of adhesion, it is assumed the front grid can survive a soldering event onto a busbar. For those front grids, a standard solar cell production line tinned copper ribbon was soldered to the middle busbars as shown Fig. 2-15c. A custom vacuum chuck holder was designed for use in an Instron, which is a well-known and standardized calibrated force meter used for mechanical stress and strain tests. The vacuum chuck and holder were each inserted vertically in the same plane as the pull force would be applied, placing more stress on the cell than in an equivalent 90 degree pull test. Once the wafer is placed on the vacuum chuck, the soldered ribbon is inserted into the pull gauge of the Instron, and the force is measured continuously as the ribbon is pulled. The ribbon will be pulled off the solar cell in one form or another, but it is also important to note the location of the ribbon tear. This is observed visually and under SEM, and bond strength between films can be qualitatively discerned. Failure of this test is deemed as <1N/mm pull force required to remove the ribbon from the solar cell. 1N/mm is defined as the instantaneous force measured, divided by the width of the soldered ribbon, which in this work is 1mm wide. Consistent measured pull force >1N/mm would be considered passing this test.

Each tested seed layer only continued to the next adhesion test if it passed the current test i.e., a solar cell with a certain seed layer that failed the initial probe test did not undergo the tape test. All Cu-SHJ cells produced in this work achieved adhesion sufficient for probing after all processing was finished. The results are recorded in Table 2-2. However, not all the seed layers passed the tape test. It was observed that the light induced plating nickel cell failed at the Ni/ITO interface and the PVD Ni, Cr and Ti cells failed at the seed layer/Cu interface.

Table 2-2. Results of the adhesion tests for each seed layer and corresponding failure point (if applicable).

Test	LIP Ni/Cu	PVD Ag	PVD Ni	PVD Cr	PVD Ti	PVD Ni + NH_4OH etch
1 Probing	Pass	Pass	Pass	Pass	Pass	Pass
2 90° Tape	Fail (Ni/ITO)	Pass	Fail (Ni/Cu)	Fail (Cr/Cu)	Fail (Ti/Cu)	Pass
3 180° Pull	n/s	Pass	n/s	n/s	n/s	Fail (Ni/Cu)

Adhesion improvement of Cu plated on PVD Ni was attempted by etching nickel oxide immediately prior to Cu plating using a dilute NH_4OH solution. The cell with the etched nickel oxide passed the tape test but failed the pull test. Thus, it was shown that stripping metal oxide is critical for adhesion of the plated Cu. The only seed layer to pass all adhesion tests was Ag, and the resulting pull test data was recorded in Fig. 2-16.

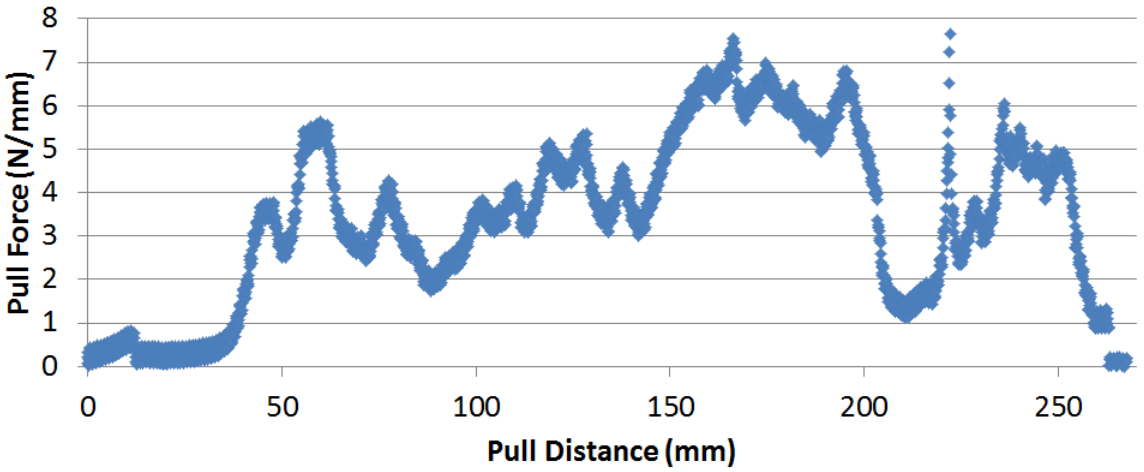

Fig. 2-16. Pull force sampled as a soldered ribbon was pulled off the busbar of a Cu-SHJ cell with a PVD Ag seed layer. The ribbon was pulled across the entire 156mm wafer, 180 degrees from the ribbon origin.

The Ag seed being the most adhered seed layer was investigated further to see the eventual failure mechanism. The image of the soldered ribbon pull for Ag is shown in Fig. 2-17 and the SEM images of several pulled fingers were imaged. The busbars where the ribbon was

pulled were too large to image in the SEM, so several fingers on the same samples were pulled instead, the fingers being only 40um wide. The SEM image in Fig. 2-17(b), (c) show different fingers with similar results. In some cases, the bond between the plated copper

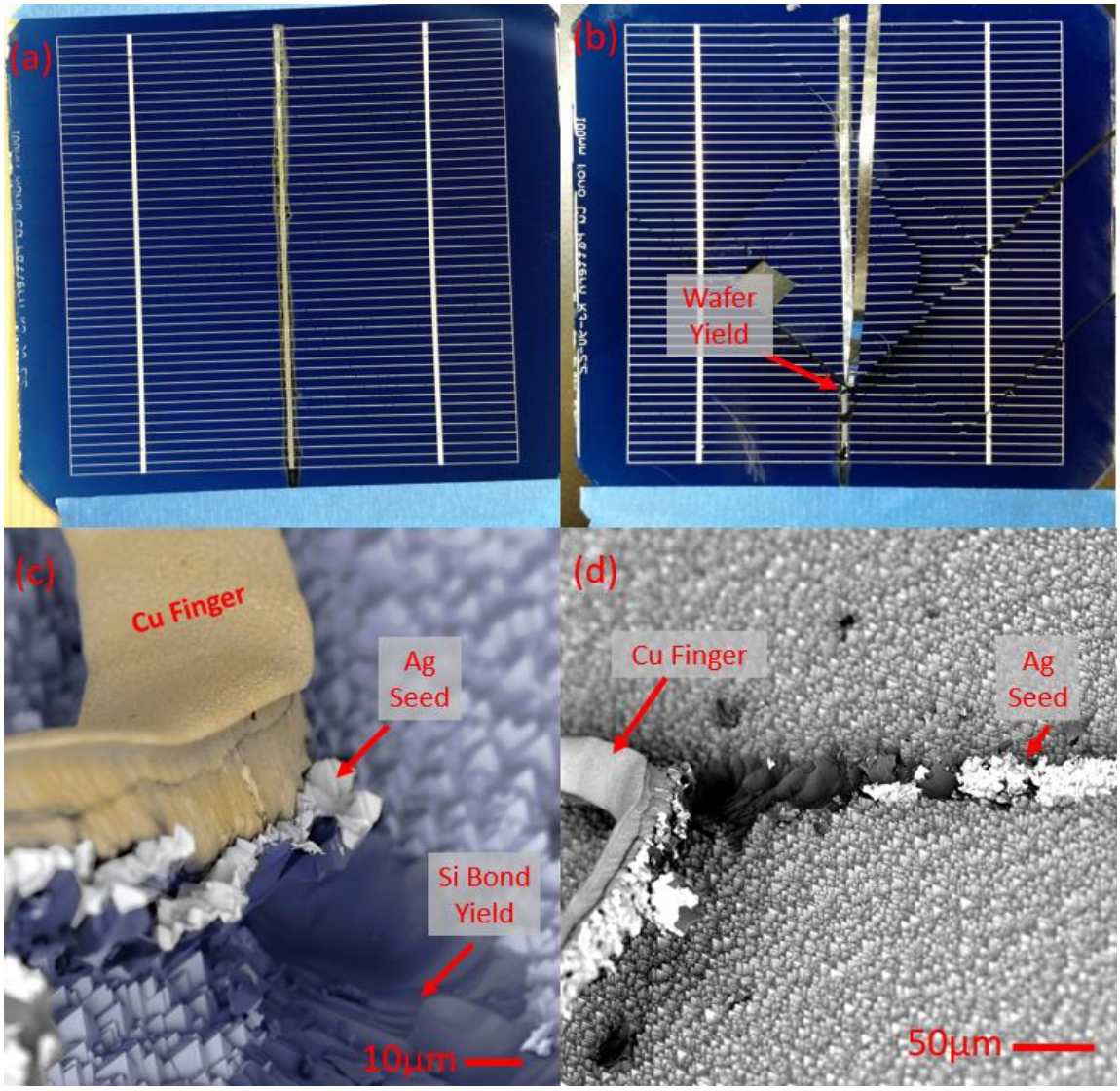

Fig. 2-17. (a)-(b) Qualitative results of the adhesion pull tests for the Ag seed layer. A full ribbon was pulled from (a) with no front grid failure and (b) with full cell failure. (c)-(d) SEM images of a Cu finger pulled from an Ag seed layer sample.

and PVD Ag is stronger than the Si-Si bonds in the wafer. The Cu-Ag bond, the Ag-ITO bond and the Si-Si bond all failed at different locations along the observed fingers. This is

an ideal scenario for adhesion, showing there isn't a limiting bond strength for the tested seed layer to the electroplated copper. The results of the Ag-Cu bond would be a standard to measure all other seed layers, but this result was not seen in any of the other seed layers in this work. Most failures for the other seed layers occurred between the seed layer/electroplated Cu interface. This was true for the seed layers that formed native oxides quickly, such as Ti and Ni. These seed layers may require a buffer layer that should be deposited in vacuum to limit the role of the native oxide growth and further improve adhesion.

2.3.4 Contact Resistance

Contact resistance is defined as the specific resistance of the interface between two different materials. The contact resistance was measured using two recipes of ITO: a higher carrier concentration n_e ITO and an ITO in a SiO_x stack configuration. The oxide stack structure is predicted to have a higher contact resistance due to the presence of the insulating SiO_x below the contacts, but the presence of this layer improves optical trapping in the solar cell structure. As such, a comparison was made for this work to see if the resistance increase from the presence of the oxide offsets optical gains.

Contact resistance was measured using the transfer length method (TLM) on an equivalent SHJ structure. The TLM structures were patterned using photolithography and outer edge isolation was attempted by abrading the surface on the edges. TLM implementation in this work is conceptualized in Fig. 2-18. By applying bias between metal bars of known dimensions and spacing, it is possible to obtain the resistance between the metal and the material to which the metal is bonded. By measuring different gaps, one can neglect the sheet resistance of any material that lies underneath the metal. If multiple

materials are stacked below the metal, the contact resistances of all these materials are combined into one measurement. It is necessary to build independent TLM structures which isolate 2 layers at a time if contact resistance is needed between each individual layer. Furthermore, parasitic resistances are present that can draw measurement current away from the interfaces which are summarized in Fig. 2-18(a). Lateral currents can flow around the contact pads, which mitigates the effects of current crowding at the contacts but gives a lower estimate of the contact resistance than if the contacts were laterally isolated. Abrading the topmost layer at the edges of the contacts, like was performed in this work is one way to force the measurement current to flow straight from contact to contact. Another measurement inaccuracy can arise when the bottommost measurement layer is not adhered to an insulating substrate. Non-zero resistance in the bulk material on which the measured films are bonded allows current to flow into the bulk instead of solely in the films. This introduces both the contact resistance and the bulk resistance of the bulk material into the measurement. Since the contact resistance between the two ITO variants may be different, it will add a different resistance value to each measurement, further complicating the measurement. The films in this work were deposited on an undoped amorphous silicon layer with a high sheet resistance on a c-Si wafer. As stated previously, only the combined contact resistance was measured in this work, so contact resistance is measured between ITO:Seed Layer:Electroplated Cu. However, since each seed layer was tested on identical structures a valid comparison can be made here.

When the contact resistance is multiplied by the area of the contact pads used in the TLM measurements, the value given is known as the specific contact resistivity ρ_c. The value of ρ_c allows for contact resistance comparisons independent of the TLM structure

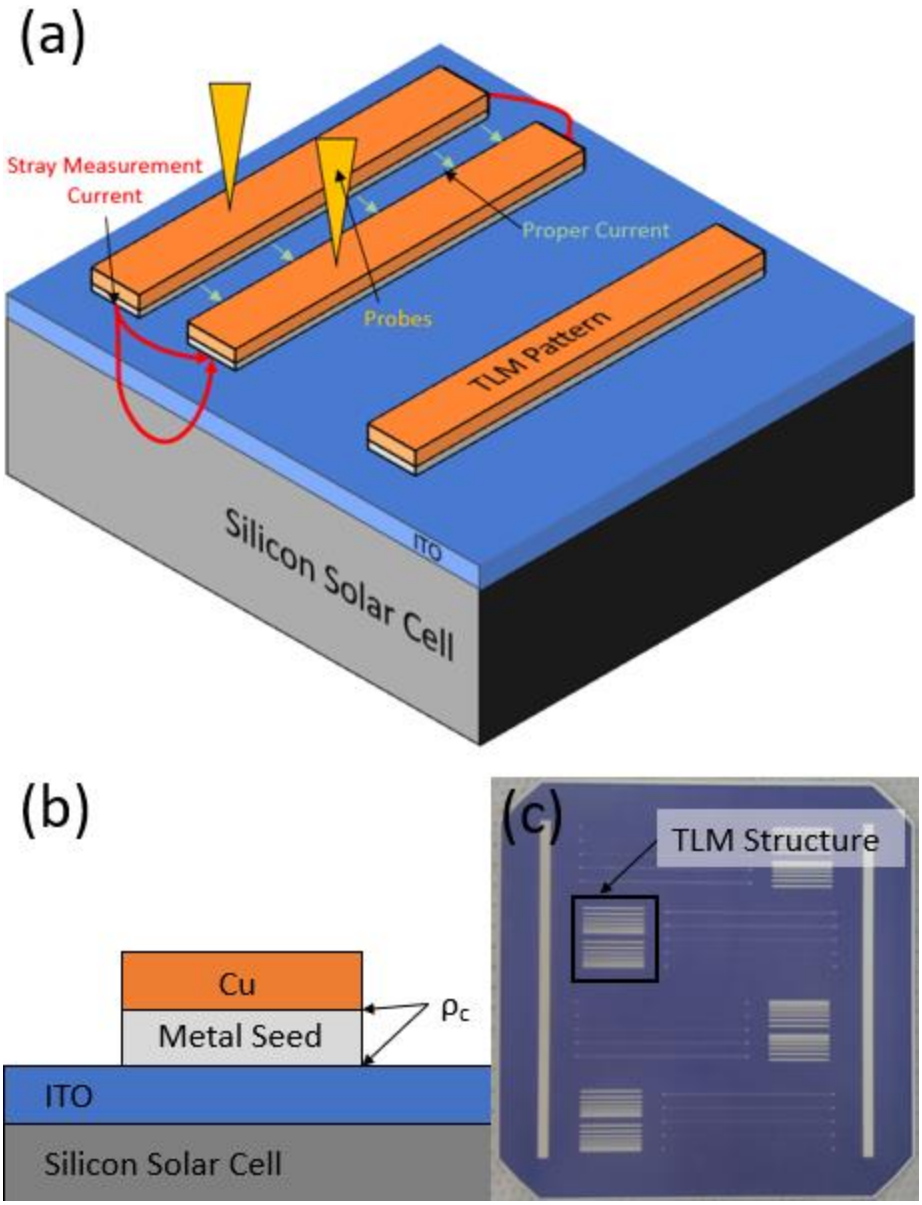

Fig. 2-18. (a) Diagram showing the TLM approach to measuring contact resistance and the possible areas of non-idealities in this work, namely the parasitic currents from outside the TLM pattern and into the silicon bulk. (b) The contact resistance was measured simultaneously for both the electroplated Cu to the seed layer and the seed layer to the ITO. (c) Image of a photoresist TLM pattern on a test wafer prior to electroplating.

pad sizes used in literature. The TLM pads remained constant in this work, so the calculation for ρ_c is redundant, but is used for consistency. Fig. 2-19. Specific contact resistivity of various metal seed layers on two different TCO layers. The specific contact

resistivity was measured using TLM patterns of the metal seed and ITO on an undoped amorphous silicon substrate. shows the specific contact resistivity of various metal seed layers on the two ITO variants. Contact resistance of 0.4 mΩ-cm^2 was achieved on the high electron density ITO and 2 mΩ-cm^2 on the ITO/SiO_x stack when using a PVD Ag. It was also found that contact resistance for Ni could be reduced 5-10 times by etching metal oxide prior to plating.

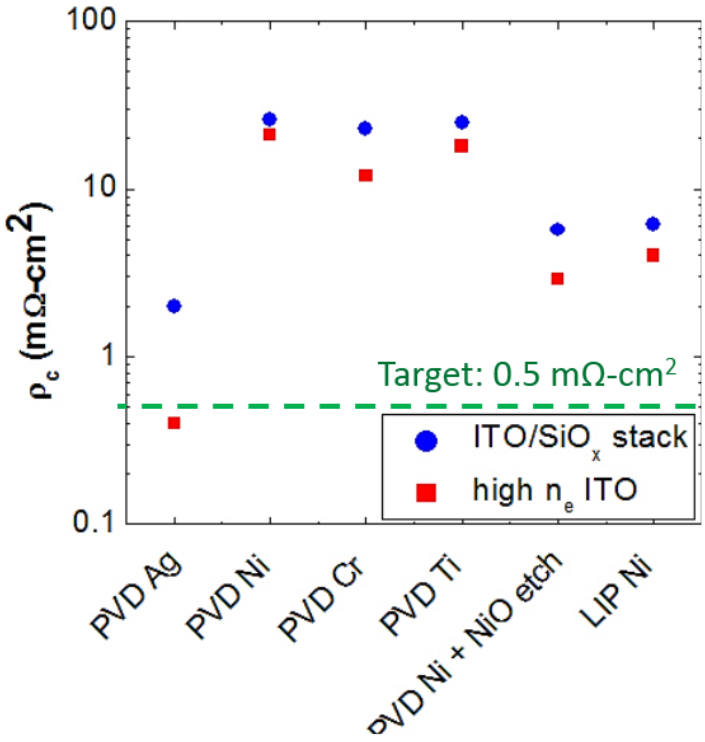

Fig. 2-19. Specific contact resistivity of various metal seed layers on two different TCO layers. The specific contact resistivity was measured using TLM patterns of the metal seed and ITO on an undoped amorphous silicon substrate. The ideal specific contact resistivity calculated in the model in Section 2.3.1 is shown here as 0.5mΩ-cm^2.

2.3.5 Line Resistance and Four Point Probe

Line resistance is a specific resistance used in solar to describe the resistance along the length of a finger on the front grid. The line resistance is a partial resistivity independent of the length of the finger, but dependent on the cross-sectional area i.e., changing the

length of the finger will not affect the line resistance value, but changing the finger width, length or material will change the line resistance value. Calculated line resistance is input into front grid geometric calculations to determine the total resistance of the front grid followed by the total series resistance of the solar cell as shown the following equation:

$$R_S[\Omega cm^2] = R_{Bulk} * t_{Wafer} + R_{Emitter} + R_{Contact} + R_{Finger}$$

Besides its necessity for series resistance calculations, line resistance can disclose much more information regarding the geometry of the fingers. Geometrically, line resistance gives insight to how square the fingers are, the aspect ratio of the fingers, and the cross-sectional density of the fingers. The effects are visually summarized in Fig. 2-20.

For identical material and aspect ratio parameters, two different line resistance values can signify a different squareness between two sets of fingers. Squareness is defined here as the ratio/percentage of the cross-sectional area of the finger profile to the area of a rectangle of similar width and height:

$$\text{Squareness} = \frac{\text{Cross Sectional Area of Finger}}{\text{Area of Rectangle with Height and Width of Finger}}$$

A higher percentage of squareness is desirable for a finger, due to a higher density of material being located on the finger. For a finger of a particular width and height, the extra conductive material from a highly square finger will lead to a lower line resistance than a finger with low squareness. Fig. 2-20a demonstrates this phenomenon. Screen-printed fingers tend toward a bell-curve shaped cross section due to the paste nature of the metal during placement on the solar cell. Mesh and squeegee pressure parameters during screen printing, in addition to drying, make it difficult to achieve square profiles. Contrast this with the electroplated copper fingers with photoresist masks in Fig. 2-20b. The rectangular channels allow for near perfect squareness of the profile, assuming growth ceases before

the top of the channel is reached. In this instance, assuming the materials were identical, the electroplated copper in the rectangular walls of the photoresist would have a lower front grid resistance than a front grid with a screen-printed deposition. For calculating aspect ratio, line resistance is typically used to derive the height of the deposition. For screen printing and photoresist patterning, the width of the desired fingers is typically well-defined. A certain screen mesh is used with specific openings for the fingers, just as a specific chrome mask is used for certain finger channel widths. In these cases, measured line resistance can be used to derive averaged height of the fingers. Since plating and screen-printing recipes can vary the height of the fingers, it is useful as a general inference to the height and aspect ratio.

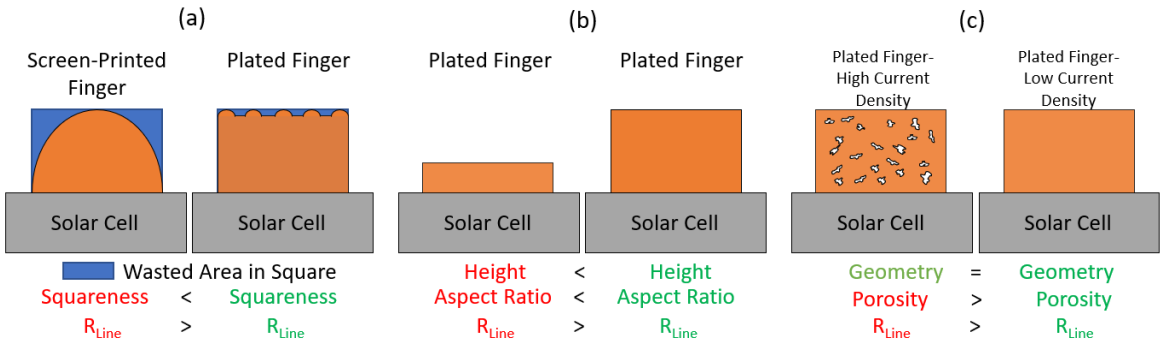

Fig. 2-20. Visual explanations and comparisons of (a) squareness, (b) plated finger height and (c) plated finger density or porosity.

For a solar cell front grid, a line resistance measurement can also give an insight into the porosity of the deposited metal of the front grid of a solar cell. Fig. 2-20c shows two fingers with identical widths and heights composed of the same material but with different line resistances. When examining the screen-printed silver of traditional solar cell front grids the organic compounds that evaporate during the firing step leave gaps in the structure of the front grid. A honeycomb like structure which was seen previously in Fig. 1-9 is what

remains. Similarly for electroplating different plating recipes can yield different porosities in the final product. High plating currents lead to large localized electric fields near the openings of the photoresist, which deplete electrolyte ions in those regions. Carrier depletion leads to a drift dominated deposition process which accelerate electrolyte ions to the depleted regions in the openings of the photoresist electrolyte ions bond to the nearest plated growth. A porous structure is what remains. Conversely, low plating currents retain the more desirable diffusion dominated plating process in which adatom growth of electrolyte metal occurs. A solid, non-porous structure is what remains from this method, resembling more of a bulk material when cross examined. Given identical cross section geometries, the same deposition process can yield different line resistance values, giving insight to the quality of the deposited structure.

The tool used in this work to measure line resistance is the four-point probe. A four-point probe is composed of four conductive pins in a line. A current is applied through the outer probes and the voltage is measured with the inner probes. In this way, the resistance of the line can be measured using the four-point probe by multiplying the applied current with the measured voltage. A four-point probe is typically used to measure the sheet resistance of a film or bulk resistance of a wafer, but if the probes are carefully applied to the top of a finger, the line resistance of that finger can be calculated as seen in Fig. 2-21. Since the spacing between the probes need to be carefully controlled in the four-point probe for accurate sheet resistance measurements, the measuring distance along the finger is quite well known. The calculated resistance is divided by the probe measuring distance to obtain the line resistance.

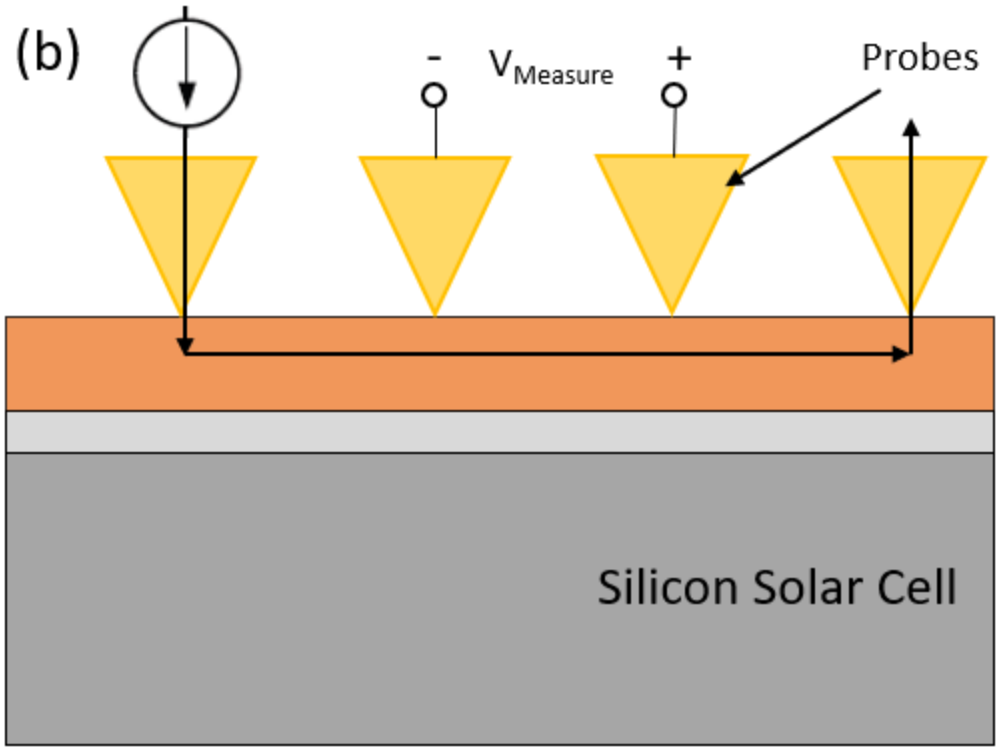

Fig. 2-21. Diagram of a four-point probe. The outer two probes supply a known current through the through each other and the inner two probes measure the voltage generated by the supplied current. Thus, a resistance can be measured. By placing the probes on the Cu finger, a resistance could be calculated.

By changing the width of the finger channels and height of the photoresist during photolithography, line resistances measured using the four-point probe can be plotted and compared. Additionally, by taking an ideal rectangular cross section of a particular height and width with the resistivity of bulk copper, one can compare the quality of the electrodeposited finger on this plot. This was performed in Fig. 2-22, which shows the measured and simulated line resistances as a function of finger width for different finger heights. For the ideal copper fingers, a 15-µm-thick Cu finger with the width of 20µm would have a line resistance equal to 0.6 Ω/cm. In addition to the measurements made in this work and the ideal copper fingers, line resistance measurements were also used from the Swiss Center for Electronics and Microtechnology (CSEM) for their copper plated

fingers and the screen-printed Ag fingers [9]. It is notable that the line resistance of the screen-printed Ag fingers was much higher at all linewidths than the electroplated copper. While the copper plated fingers of any height in this work exceeded the line conductance of a high-quality finger recorded from CSEM, the target of 0.5Ω/cm predicted by the model was only reached with the 20-35µm tall fingers. Thus, to fully exploit the benefits of the copper plated front grid, the tallest fingers the photoresist allows should be plated. As shown earlier, only the dry film photoresist could achieve 20um tall features, so this photoresist was used for the final cell development.

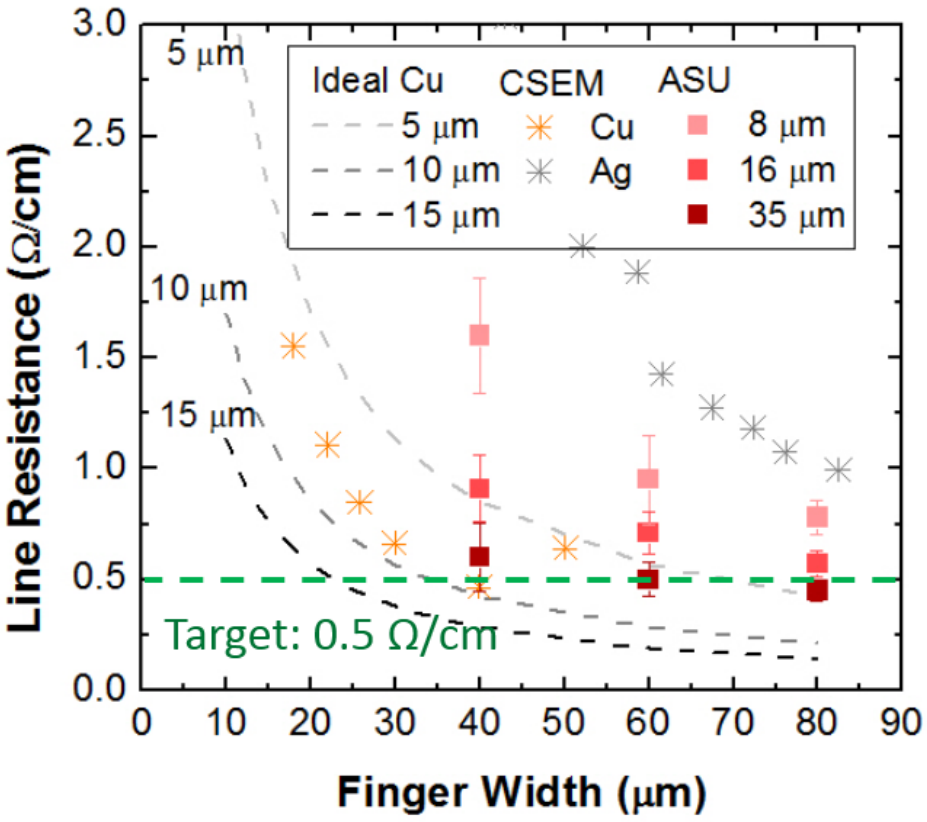

Fig. 2-22. Line resistance of plated copper and screen-printed silver fingers of various heights. Dotted curves are ideal copper plated lines with a perfect rectangular profile throughout the line. Dotted curves represent the minimum line resistance possible for a plated line. CSEM and ASU data points represent the plated fingers of the Swiss Center for Electronics and Microtechnology and the author respectively.

2.3.6 Full Cell Results

Table 2-3 shows the results of the optimized 100 cm^2 cells plated using the different methods studied in this work. All different plating and patterning methods produced the cells that can achieve more than 20% efficiency. The record cell patterned by the spin-on

Table 2-3. Parameters of the best Cu electroplated SHJ cells produced in this work.

Plating Type	Mask	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	Eff (%)
EP	Printable photoresist	728	37.9	76.2	21.0
EP	Spin-on photoresist	729	38.5	78.0	21.9
EP	Dry film photoresist	731	37.7	76.5	21.1
EP	Dry film photoresist**	-	-	-	21.7
LIP	Screen printable photoresist	728	35.6	76.0	19.6
LIP	SiO_x mask	729	36.1	76.1	20.0

** NREL certified 156mm solar cell

photoresist achieved 21.9% efficiency. It should be noted that this cell was made on a 180-µm-thick wafer in order to get a higher pseudo FF (which allowed to increase FF) and J_{SC}, whereas the other cells were made on 120-µm-thick wafers. The record cell also had 30-µm-wide fingers leading to lower grid shading, which contributed to 0.5 mA/cm^2 higher J_{SC}. Thus, the efficiency of ASU's record Ag screen printed cell was increased by 0.4% absolute.

Also, cells on 5" wafers with full wafer Cu grids having 2 busbars and 60-µm-wide fingers were produced. The best cell made on 180-µm-thick wafer achieved 21.9% efficiency. Figure Fig. 2-23 shows the photo of the record cell as well as PL and EL images highlighting overall uniform plating and various edge losses limiting cell performance. The parameters of the best 5" cell were V_{OC}=732mV, J_{SC}=38.4mA/cm^2, FF=77.9%.

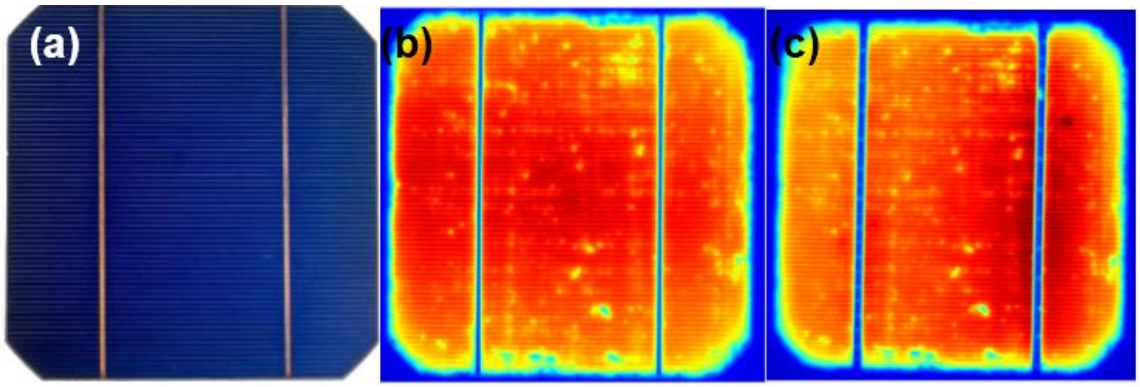

Fig. 2-23. (a) Photograph of highest efficiency 5” Cu-SHJ solar cell produced, with corresponding (b) photoluminescence and (c) electroluminescence images of the cell in (a).

CHAPTER 3

LOCALIZED ELECTROPLATING METHODS

Since its inception, Localized Electrochemical Deposition (LECD) has proven to be an effective method of plating high aspect-ratio and complex three-dimensional microstructures without the need for expensive masks [68]. These structures are created using a micro-anode, typically made of platinum (Pt) wire, coated with a dielectric that has been polished to expose the Pt tip. The potential at the micro-anode draws the metal ions in the electrolyte to the region under the tip, forming a metal pillar on the substrate beneath the tip [69], [56]. Variations in setup complexity allow for creating anything from metal pillars grown normal to the substrate, to three-dimensional growth patterns such as coils and bridges [70], [71]. Alternatively, plated lines have a more immediate and widespread use in the electronics and semiconductor industries as busbars and contacts. Therefore, creation of certain line configurations displayed in this work could lead to more cost-effective plating solutions for these industries. However, direct translation of this technology to fabricate large area patterns on substrates is challenging since the plating area is defined by the size of the anode, which in these cases is on the scale of tens of microns [68]. Plated lines have been created using different variants of the LECD method [72], [73], but plating setups for high aspect ratio plated lines may be difficult to scale due to the head positional accuracy and plating time. Additionally, to create the high aspect ratio and complex geometric structures for which LECD is known, stepper motor and feedback systems are required to move the micro-anode and dampening systems are used to mitigate shifts in the anode movement [68]. LECD differs from traditional plating by means of the electrochemical parameters. As stated previously, inert anodes such as Pt are

used instead of anodes composed of the metals found in the plating electrolyte, which in this work is copper (Cu) [68]. The inert anode, being insoluble in the bath, induces a different reaction than what is seen using a Cu anode [74]. The decision to use an inert anode for previous LECD research is necessary, as the anodes seen in all LECD work are significantly smaller than the cathode. The high dissolution rate caused by the low anode/cathode exposed surface ratio would dissolve or disfigure a Cu anode before an LECD structure forms. The consistent shape and location of the anode are critical in LECD to create consistent plated structures. It is theorized that a larger exposed surface area on the anode, such as the anodes used in this work, would lead to a more controlled dissolution of the Cu anode, hence the decision to use both inert anodes and Cu anodes in this work. This novel variant of LECD is presented and named in this work wire LECD (WLECD) and uses anode wires run parallel to the substrate.

The LECD performed in this work diverges from all previous variants by the orientation and application of the anode wires. Instead of a coated anode wire with an exposed tip perpendicular to the substrate, as in Fig. 3-1a, the anode wires are strung parallel to the substrate, as in Fig. 3-1b. In this configuration, plating occurs locally under the entire length of the wire, and not just the tip, creating an LECD line on the cathode. Consequently, electroplated wires, or rows of electroplated wires of arbitrary lengths could be plated simultaneously to create custom grid patterns. The continuous plating along the anode wire negates the need for a complex micro positioning system seen in other LECD work to create the same plated lines. However, there are some challenges, including but not limited to wire uniformity and cathode surface flatness/parallel with wire, which are discussed in this work.

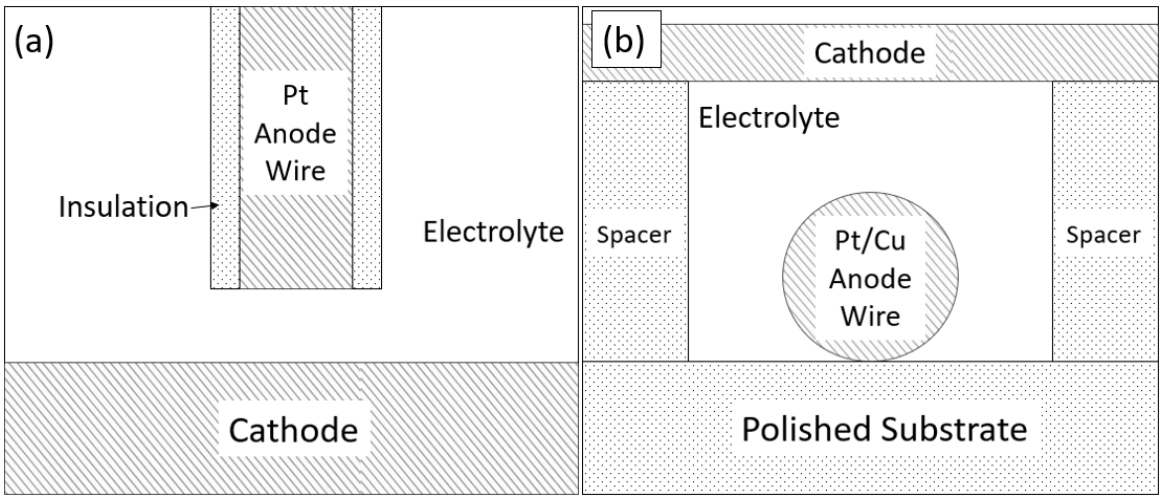

Fig. 3-1. Diagrams showing cross section views of (a) a typical LECD application and (b) WLECD used in this work. For this work, (b) depicts how the WLECD anode wire is fully exposed and flush with the surface of the polished substrate to maximize parallel with the cathode. Typical LECD processes in (a) sheathe the anode with an insulator and expose the tip normal to the cathode.

There are several advantages and disadvantages of this method over traditional LECD for depositing fingers. The first advantage, a lack of moving parts, means complex machinery is eliminated. Second, plating time for a finger or line is significantly reduced compared to traditional LECD due to continuous plating along the anode wire. There is no need to plate individual spots to create the line with the LECD microtip as shown by some in literature [72]. Some disadvantages of the technology include the complexity of wire stringing, cathode surface flatness/parallel with wire, and anode materials. Stringing the anode wire requires enough tension to keep the wire taut during plating without deforming or snapping the wire. Depending on the material and the forming process, different materials may be more difficult to accomplish this with due to changes in tensile strength. Cathode surface alignment was performed in this work with spacers and substrates of known flatness (silicon wafers). While this introduced a known flatness, it did not give a known parallel. As such, alignment for this technique is extremely difficult, and an

important consideration moving forward. Finally, this process is limited to the available materials capable of being forged into wires. Limitations on rolling and other production techniques translate to minimum wire diameters of tens of microns (with varying diameter tolerances along the wire). The scale of the tensioning devices used in this work further limited the minimum wire diameters to 70μm to minimize wire breakages during tensioning.

Due to the high-aspect ratio capabilities of LECD without the use of any sort of masking mechanism, it seems to be an appealing process to integrate into SHJ front grid plating technologies. Current masking methods (shown in this work), when used with plating, create a “mushroom” phenomenon that forces the front grid pattern height to be limited to the height of the mask. This would not occur in LECD due to the mask-free nature of the process. Also, despite Cu plated SHJ cells achieving lower utility and residential LCOE than traditional Al-BSF cells, photolithography represents 40% of the costs of an SHJ production line [13]. With no limitations on grid height and the possibility of complete elimination of precious metals, a mask-free process such as LECD seems the next logical step for Cu plating technology on SHJ solar cells.

3.1 OPTIMIZATION OF COPPER-PLATED FRONT GRID PATTERNS

Currently, the predicted trends of Ag-Screen printed fingers push the resolution of such lines to well below the 40um mark. The ITRPV predicts the resolution of such lines to be less than 20um in 2030, with current industry linewidths rivalling 40um [6]. Linewidth is an important parameter to control, as it defines the conductiveness of the front grid as well as the optical shading of the cell. Ideally, the linewidth of the finger should be as small as possible while also being as conductive as possible. Since metals are opaque, they absorb

and reflect photons. Photons that interact with the front grid can either be absorbed by the metal (loss), reflected by the metal and transmit out through the glass (loss), or reflected by the metal and glass and absorbed in the solar cell (gain). Thus, any area covered by metal on the front of the cell is a dead zone for carrier generation. Modern cells have reduced shading of front grids from 15% of first- and second-generation solar cells to about <7% with advances in paste and screen technologies [75]. While this reduction is noteworthy, since incoming light directly translates into module power, every percent lost to shading is significant. Making the front grid more conductive can be achieved several ways. This first is to simply widen the fingers. Wider fingers create a less resistive pathway for carriers to travel, but also increases the shading losses. 2) Make the fingers taller. Taller fingers give the same conduction increase as widening, but since the expansion is normal to the cell surface, it incurs no additional shading losses. However, the height is usually fixed due to technology and process limitations. 3) Change the conducting medium. This is more difficult to implement, but electroplated copper is 3-4x more conductive than the screen-printed Ag paste used in industrial screen-printing pilot lines [37]. 4) Decrease the finger length. The total resistance the carrier experiences increases proportionally with distance. Industrial solar cell manufacturers heavily utilized this method to reduce finger series resistance by adding more busbars that are thinner, so shading remains constant. Fig. 3-2 shows the change from 2 busbars to 5 busbars, with state-of-the-art industrial cells boasting 12 busbar patterns. However, this increases the complexity of the stringing process and can only be optimized so far as cells increase in size. Therefore, the goal of the modelling should be to minimize the front grid coverage while also maximizing conductivity of the front grid using the four methods stated above.

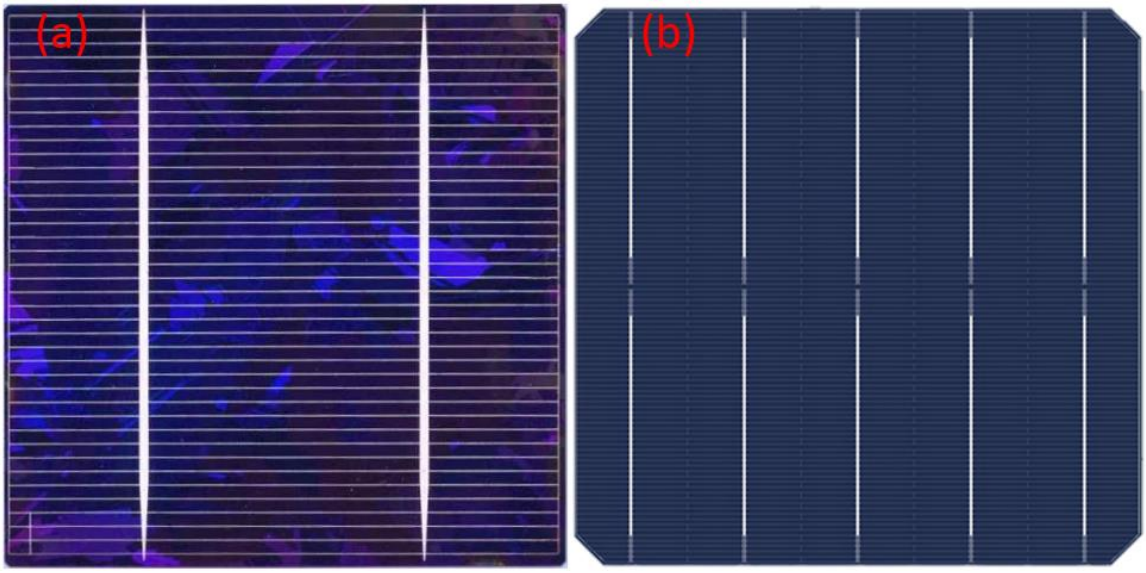

Fig. 3-2. Solar Cell busbar patterns from a (a) first generation 2 busbar cell and a (b) more modern 5 busbar cell.

Another point to consider is the future of solar cell geometry and cell design. Cell dimensions and busbar technology are changing quickly in industry to reduce efficiency losses and offset costs. The ITRPV predictions in Fig. 3-3 show half cells and 6 busbar/busbar-less technologies to have a dominant market share within the decade. This creates new avenues for cell design. Due to the high conductivity and differing process parameters of electroplated copper vs screen-printed Ag, a more unique and robust front grid can be modelled. For example, electroplated copper can have much longer fingers than that of screen-printed Ag, meaning the same or better efficiency could be achieved with a shingled front design. This would reduce processing costs associated with stringing cells in modules. Therefore, rather than compete with classic industry standard H-Bar pattern, in this work we will examine future standard designs. In addition to the contact method, the dominant market cell size is predicted to be half and quarter cells by 2030. The reason

for this move from full size cells is the cell-to-module (CTM) power ratio. Reducing the cell size reduces current losses in the module when keeping cell efficiency identical.

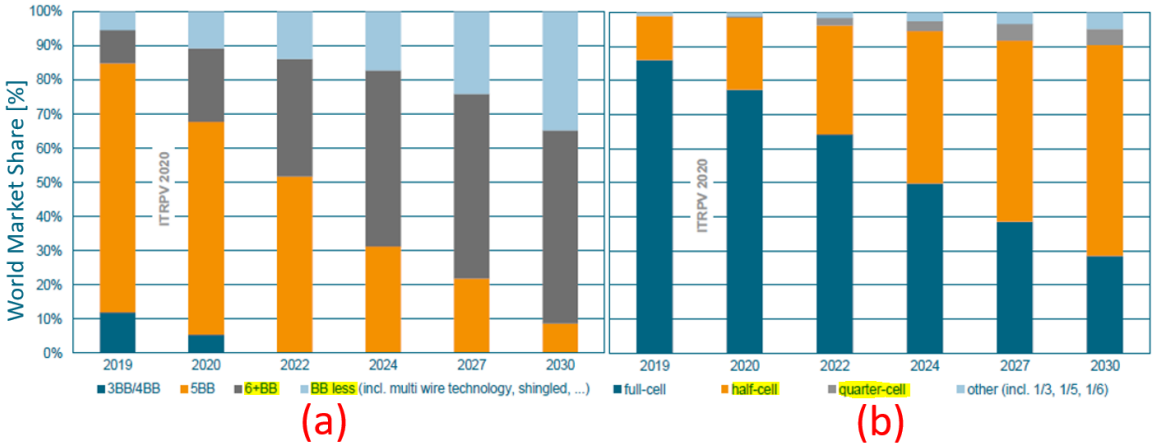

Fig. 3-3. Predicted trends of solar cell development to 2030 for (a) number of busbars per cell and (b) solar cell sizes used in modules. The trends show increasing the number of busbars and the elimination of busbars for future cell designs, as well as an industrial preference to dice solar cells in half rather than stringing full cells in a module [6].

As screen-printed Ag finger width decreases to 20um, busbar quantity and finger height must increase to maintain conductivity, else resistivity losses will offset optical gains. The number of busbars present on first generation solar cells was 2, and today that number ranges anywhere from 6-12, depending on the manufacturer. While it is possible to increase busbar quantity beyond this, challenges and costs associated with stringing large number of ribbons per cell in modules will eventually reach a tipping point. This is where it becomes advantageous to adopt a multiwire or shingled design, both of which hold conductivity challenges for 20um screen-printed Ag in a full or half-cell format. Conversely, electroplated copper would adapt well to these technologies for current and future cell sizes. This adaptation would also have other benefits, such as increasing CTM efficiency (shingled cells have no gaps between wafers), but only individual cell efficiency is explored in this work.

For this work, a 156mm silicon heterojunction half-cell was modelled using a PV cell simulator called Griddler, with a 6BB Ag screen-printed front grid as well as a 1BB shingled copper electroplated front grid as can be seen in Fig. 3-4 [76]. Current was

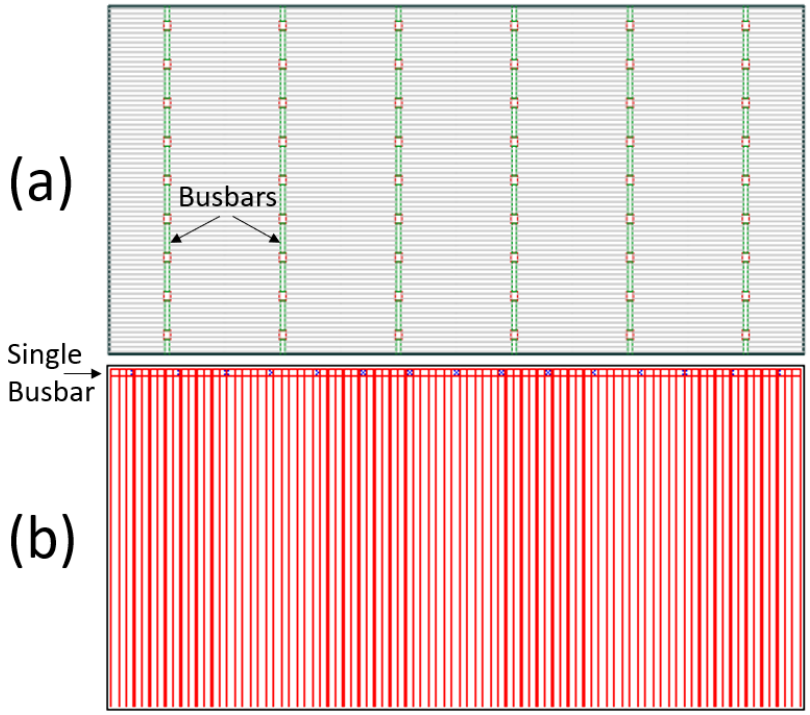

Fig. 3-4. Model graphic for a (a) 6BB Ag screen-printed half-cell and a (b) copper-plated single BB shingled cell. Model color variations from (a) and (b) are due to program inconsistencies with imported CAD files in Griddler. The fingers run shorter and are horizontal on (a) while they run across the entire cell vertically on (b). Finger spacings for (a) and (b) were optimized for highest efficiency in the respective model.

extracted at individual points along the busbars for the 6BB cell and along the edge for the shingled busbar. Finger spacings were not identical for each; they were optimized based on the finger width limits of each technology and the location for current extraction (busbar location and count). The optimizations were performed using PVeducation's front grid series resistance/shading modeler when total efficiency losses were minimized. The front grid heights were fixed to 20um tall, which is the standard height of the screen-printed

front grid. Despite there being no limit to the height of an LECD front grid, plating heights did not exceed this value for this work. Besides the front grid, all other parameters such as cell geometry, SHJ structure, voltage, and series resistances (contact, emitter, bulk, etc.) were identical. Table 3-1 shows the values for the front grid and emitter.

Table 3-1. Parameters of each solar cell design to be calculated in Griddler.

Cell Type	Emitter Sheet ρ (Ω/sq)	Finger Sheet ρ (mΩ /sq)	Line Height (μm)
Screen Printed Ag (Half-Cell)	100	2.5[1]	20
Cu Plated (Half Cell)	100	0.85	20
Cu Plated (Quarter Cell)	100	0.85	20

[1]Data used from [37].

The modelled data shows it is possible to have balance of front grid series resistance and optical losses that result in a next-generation copper plated shingled half-cell having higher efficiency than the screen-printed counterpart as shown in Fig. 3-5. For the parameters listed, Cu-plated quarter cells have negligible efficiency differences up to 75um line widths and exceed the efficiency of screen-printed cells at 55um. Considering the half-cells, 40um fingers would also be within a 0.2% efficiency difference with the screen-printed Ag half-cells. The efficiency values shown here in the modelling section highlight the feasibility of these cu-plated front grid designs that are better suited for LECD plating.

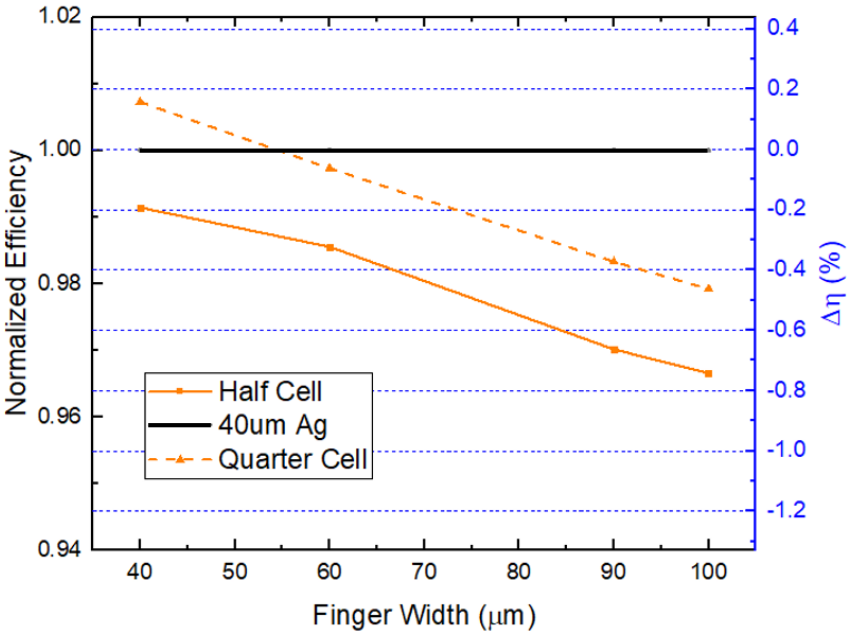

Fig. 3-5. Plot comparing the simulated efficiencies of the copper-plated half and quarter-cell with the simulated Ag screen printed solar cell. Efficiency accounts for series resistance losses and optical losses from shading of the front grid. Normalized efficiency is the fractional percentage gains/losses of each technology compared to the Ag screen-printed solar cell while the delta translates this to actual gains/losses.

3.2 EXPERIMENTAL SETUP

3.2.1 WLECD

A commercial Cu sulfate bath with brightener is used here, along with a custom 3D printed bath housing for experiment set up. The bath contains a center tank, wire tensioners, and busbars to make contact to the anodes. Pt and Cu anode wires were each suspended on the polished substrate surface and tensioned to maximize flatness across the substrate. For this work, the active plating wire length shown in Fig. 3-6 was 1cm along the substrate, where active length refers to the length of wire lying over the gap where solution is circulated. The substrates are longer than this active length, and thus plating occurs out of this active length, but the only well-defined anode-cathode distance is in the center and on

the polished substrate. For experiments requiring circulation, a peristaltic pump was used to push solution through the center gap and to the cathode face.

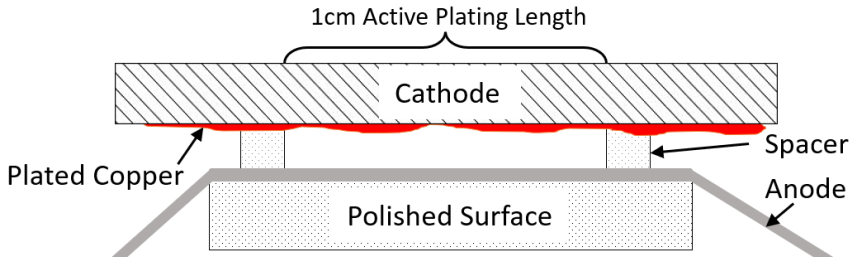

Fig. 3-6. Cross section view of WLECD. Active area is defined as the region where the anode-cathode spacing is set by the spacers and where reliable measurements were taken in this work. The wire is tensioned laterally over the polished substrate by a custom tensioning system extending out of the diagram at each end of the anode wire (not shown). Diagram is not to scale.

The Cu wires were polished and had a diameter of 78µm +/- 2.5µm, and were made of 110 grade Cu. The platinum wires had a diameter of 76µm and had a purity of >99.99%. Two types of cathodes were used in this work. The first were brushed brass substrates of hull cell quality. These substrates were used for most plating experiments and analysis due to ease of electrically contacting the rear side of the substrate, which was necessary for the WLECD setup used in this work. The second cathode types were single side polished, highly doped (0.001-0.005Ωcm) silicon wafers with a physical vapor deposited (PVD) sputtered silver (Ag) seed layer. These substrates were used for scanning electron microscope (SEM) imaging to distinguish Cu seed deposits from the background. The brass cathodes underwent an acetone wash after the manufacturer protective coating was removed, followed by drying with nitrogen. The silicon samples were cleaned in the order of RCA-B, Piranha, and a buffered oxide etch to remove the silicon oxide prior to PVD Ag sputtering. The spacers used in this work are made of solar grade silicon that had undergone a wet-etch in an 80C potassium hydroxide (KOH) bath. Wafers were processed with

different times to achieve desired thicknesses. Wafers were then cleaved to small pieces and thicknesses were measured on a polished stone surface with a digital micrometer in several places on each spacer.

Prior to plating, the anode wire was strung through the bath, over the polished surface and externally contacted to a busbar on the opposite end of bath (see Fig. 3-7). Each anode wire was then individually tensioned using a dedicated compression spring. The spacers were placed on the polished substrate and the tank was subsequently filled with solution. The cathodes were adhered with silicone to a holder containing a spring probe contacting the rear of the cathodes. Plating current and voltage were controlled and monitored by programmed Keithley 2400 power supplies at a computer terminal. Since the anode/cathode gap is static for this work, plating would commence for a specified time or when a short occurred, whichever the experiment dictated.

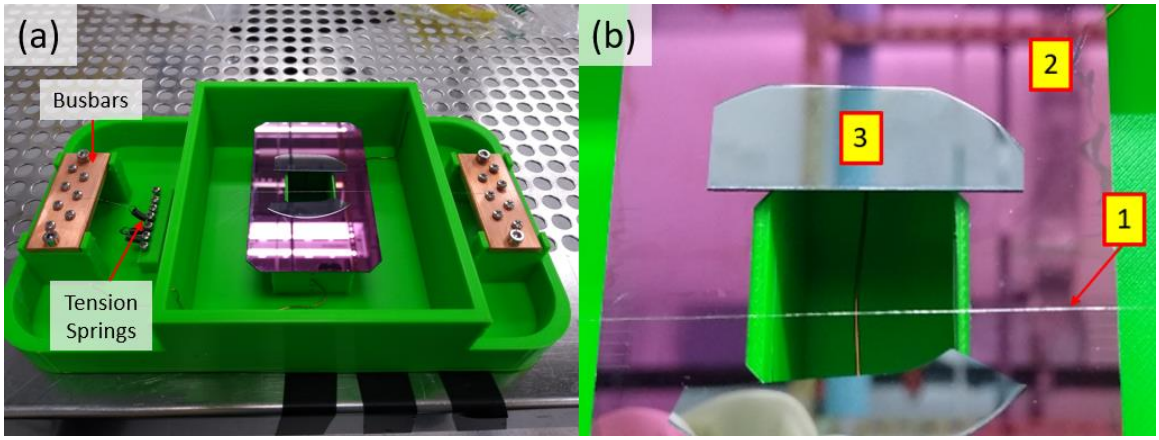

Fig. 3-7. (a) The physical plating setup, without electrolyte and (b) a close-up of the center plating active area. (a) Center of tank is filled with solution and cathode wafers are placed face down on the spacers. Labels in (b) are shown as (1) anode wire, (2) polished flat surface, and (3) spacer.

3.2.2 LECD with Large Area Anode

The OFC Cu anode underwent photolithography for H-bar front grid designs and lines of widths ranging from 20um to 100um. The cathodes used were sheets of polished brass as well as a solar cell with an ITO layer and 200nm of sputtered Ag on the surface. Fig. 1-7 shows this setup. The anode and cathode were spaced 30um apart in solution and plated. Cu ions sourced from the anode would plate locally underneath the openings of the cathode. At a larger anode/cathode spacing, plating would be more uniform on the surface, but since the openings are much closer to the cathode than an adjacent opening, localized plating can occur. Due to the nature of the setup, any oxygen trapped between the openings of the mask would remain and would interfere with plating. Thus, this wasn't be performed with the inert Pt anode.

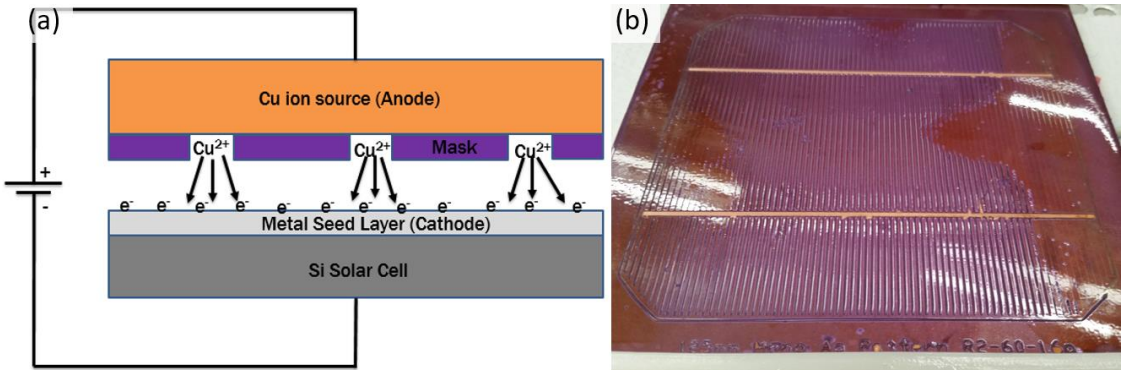

Fig. 3-8. (a) Concept of LECD using a large area patterned anode and (b) the H-Bar photolithography patterned OFC large area anode. The anode source is masked so copper is selectively corroded from the anode in areas defined by the mask. Minimization of the anode gap leads to concentrated electric fields where the pattern is exposed, making preferential copper deposits under the exposed sites.

3.3 MODELLING OF LECD AND WLECD TECHNIQUES AND MECHANISMS OF ELECTROPLATING

The WLECD method of electrodeposition has been presented for the first time in this work. WLECD is a derivative of the LECD technique but differs in application. Modelling has been performed extensively with LECD techniques, and simulations of various anodes and growth structures are abundant in literature [77], [78], [70]. Of note, electric field growth simulations are particularly useful for determining plated profile shapes using LECD. The electric field growth models in literature typically use a finite element method (FEM) to calculate the electric field in an environment with a shaped anode and cathode. The simulation is iteratively solved based on the electric field value found near cathode. For the first iteration, the cathode is selected to be a flat ground plane while the anode is a rectangle with the dimension of the anode wire being used in the experiment. The electric field is analyzed after the FEM potential analysis is completed, and a simulated profile is generated from the electric field curve. As stated previously, this profile resembles quite closely the shape of the actual LECD plated structure in literature. The reason for this is that electric potential and geometry play critical roles in electroplating. With a constant electric potential value, system geometry will drive the plating deposit formations i.e., cathodes closer to the anode will plate more and sharp points will lead to higher plating density. A sharp point on a cathode will plate thicker deposits of copper, just as a sharp point on an anode will produce stronger electric fields that drive more ions towards the cathode regions closest to it. This localized phenomenon is what defines the LECD deposition environment. In LECD, a very small anode relative to the cathode is used to guide localized deposition on the cathode in the region directly under the anode. Overall,

the modelled deposition resembles what is plated in LECD. A comparison is also made between simulated and actual plated WLECD structures in this work. A low plating potential was used with the WLECD setup in this work and the results are compared with an FEM simulation with similar properties to display the efficacy of the model in these scenarios. Due to the generalized accuracy of these models in literature, this method was performed in this work; an FEM model was created here to compare possible geometries for future WLECD work and to compare modelled WLECD structures with similar structures using an LECD equivalent scenario.

To fully understand the model, it is important to review the different mechanisms driving electroplating in an electrolyte, namely diffusion, migration, and convection [79]. They are each governed by different electroplating parameters and can all be present at once in a plating bath, but the presence of all three complicates the bath to a degree that may not be possible to simulate. For simulations, it is best to limit the presence of each mechanism in the electroplating bath, although this is not always desirable or possible.

Convection is an example of difficult to simulate but a desirable plating bath mechanism. During plating, electrolyte ions can deplete near the cathode as they are deposited. Electroplating potentials that are too high will lead to this depletion, as the carriers cannot migrate through the electrolyte as fast as they are being deposited. It is therefore desirable to have a convection current, in the form of bath agitation to physically mix the solution. High agitation can replenish ions quickly near the cathode which can allow for higher plating rates in industrial applications. However, simulating convection mechanisms in an electrolyte is extremely complex, and many bath parameters must be calculated beforehand, including additive concentrations, temperature, ion mobilities,

plating current densities, and liquid flow dynamics, including laminarity of flow to name a few. These parameters are unique to each bath and must be calculated individually, making simulating a very difficult process. Due to the type of modelling desired in this work with electric field growth, optimized plating rates are not required. As such, convection driven current in the bath is assumed to be zero, and bath agitation is not performed in the WLECD work for the simulation comparisons.

Despite the critical importance of the electric field on plating, diffusion is the more desirable driving force behind plating. There is a maximum velocity that ions can diffuse through the electrolyte, depending on, but not limited to the temperature, concentration of copper sulfate in the bath, and the presence of specific additives in the bath. If too high of an electric potential is applied to the anode, ions may increase in velocity and dissolution/plating of the anode/cathode will become more non-uniform. Larger potentials intensify the difference between high electric field points and low electric field points e.g., sharp peaks or flat surfaces on the cathode respectively. In literature simulations, the electric field could be several orders of magnitude greater on a sharp point than on a flat surface in larger potential simulations [80], [74]. The stronger electric fields from the higher potentials draw a larger concentration of copper ions to electric field-sensitive points on the cathode. The migration of copper ions to these regions depletes the copper ions elsewhere near the cathode where the field is much weaker. The velocity limitations of the bath severely limit the diffusion mechanisms by preventing proliferation of the copper ions elsewhere on the cathode. The large fields continuously draw ions to the growing peaks on the cathode in a positive feedback loop. This regime of plating is known as migration, due to the electric field driving the dissolution/deposition locations. Migration deposition

produces porous deposits, rough finishes which is known colloquially as “burning” and uncontrolled deposition, all of which lead to worse deposit properties and are considered “undesirable” [81], [82]. In Section 2.3.5, of this work, the line resistance of the fingers was worse than that of the measured fingers from CSEM, most likely due to the plating recipe differences and the likelihood of more porous deposits. Despite the apparent similarities with LECD and a drift based electroplating deposit, LECD as with all plating, produces more desirable deposits when operating in a diffusion-based plating regime. One of the notable aspects of localized plating processes such as LECD and WLECD is that the anode is orders of magnitude smaller in scale than the cathode. It is by this method that the localized electric fields are produced which drive plating to the region under the anode. The goal of LECD is to guide copper ions directly under the anode and nowhere else on the large cathode. By making the anode very small and moving it very close to the cathode, the anode/cathode surface area ratio becomes very small, meaning the effective deposition area of the anode decreases to a very small area on the cathode. It is not by electric potential that the copper ions are drawn to the select region of the cathode but by the geometry of the system. If the electric potential is low, copper ions may diffuse evenly, but remain localized under the anode, whereas if the potential was high, the migration-based mechanisms would quickly guide copper to bond near the edges of the anode and the center would become porous. For the applications in this work i.e., solar cell front grid plating, full infill and not a porous structure is desired. In summary, low plating rates via lower applied potentials in electroplating and in guided localized deposition methods such as LECD and WLECD, lead to desirable front grid structures in solar.

The Nernst equation provides the means to calculate ion flow through the bath, but finding bath parameters is difficult, unreliable, and unique to each bath. Work has been done on solving the Nernst equation for LECD purposes, but the baths used were composed of $CuSO_4$ baths with different additive levels and composition [82]. These parameters would not translate to the bath used in this work, nor was the methods of finding these parameters achievable in the scope of this work. Thus, diffusion and migration transport equations for the bath could not be simplified and solved for in a model that would translate to an effective representation of the WLECD plating. Instead, an empirical method using electric fields to simulate deposit growth was utilized in this work.

Electric field models are useful for determining the approximate growth profiles of localized plated structures as seen in this work and in literature. However, there are also limitations to their use. The first advantage is that electric field models are simple to establish. They can be run without any parameters of the electroplating medium. However, this only holds true when executed in a specific electroplating regimes and situations. Additionally, several assumptions must be made about the plating process for the model to work. First, it is assumed the geometry and thus the electric field is the guiding force behind preferential copper deposition. This is the case for shaped anodes or high electric field electroplating such as in an LECD configuration and would be undesirable in a setup meant for producing conformal electroplated films. Migration current density has been empirically found to be proportional to electric field strength and inversely proportional to the distance from the anode to the cathode, so this holds true [83]. Second, it is assumed there are always enough copper ions present in the solution where plating occurs. Apart from the final growth phases in the model where the electric field magnitude becomes

extremely large, the ideal bath scenario of ever replenishing copper ions in solution is a reasonable assumption when operating with lower electric potentials. Lower plating voltages equates to lower plating rates, which means the plating rate can ideally be less than the ion diffusivity in the bath. Finally, electroplated copper layers occur in 5μm sheets on the cathode instead of adatom deposition. Due to the limitations of numerical modelling, infinitesimal growth of copper on a cathode is not viable. Simulations were performed to compare a 20μm growth with 1μm, 2μm, 5μm, and 10μm growth increments, and a negligible difference was found between the 1, 2, and 5μm simulations. Thus, 5μm was found to be a sufficiently small building block for growth in the simulations.

As explained in Section 3.6, many non-idealities occurred with the wire process. Thus, a new method was proposed which involved encasing the wire anode in epoxy and exposing the wire in electroplating solution. This method would theoretically mitigate the stray electric fields as well as inconsistent plating events seen in the previous section. While not physically demonstrated in this work, it was modelled along with the bare WLECD and LECD method to compare plated geometries.

3.3.3 Geometry and Electric Field Growth

The three geometries modelled in this work are shown in Fig. 3-9. A 15μm LECD anode, 50μm bare wire anode, and a 50μm coated epoxy wire anode are shown in Fig. 3-9(a)-(c) respectively. The geometry was chosen for each technology based on actual representations of LECD in literature and WLECD in this work. One of the smallest diameter wires reported in LECD experiments is 15μm. In WLECD, the wires needed to be tensioned to maintain rigidity, and the thinnest wires that could be tensioned without snapping were

50µm in diameter. The WLECD wire coated in epoxy was also set to 50µm and ground flat, since tensioning may be necessary while coating with epoxy and the wire needs to be exposed to generate the electric field. The geometries examined here are by no means the limits of LECD and WLECD technologies. For the 2D FEM simulations, regions of applied electric potential needed to be chosen to generate the electric field. These regions are shown in red in Fig. 3-9. For LECD, the vertical wire in Fig. 3-9(a) is coated in epoxy many times the thickness of the wire so only the exposed surface of the wire is simulated, instead of the wire sides. The epoxy thickness in this case so large relative to the anode wire size, the electric fields generated from the anode wire sides were calculated to be negligible. For the exposed anode wire in Fig. 3-9(b), the entire cross section is engaged in the plating process due to the absence of any insulating coated. Finally, the epoxy coated WLECD wire in Fig. 3-9(c) is coated with a thin layer of epoxy and sanded to expose the surface of the anode wire. For this model, it was assumed the sanding would occur halfway through the wire so the diameter of both WLECD wires were comparable. Additionally, the epoxy coating was much thinner than that of the LECD coating, so modelled electric potential was applied

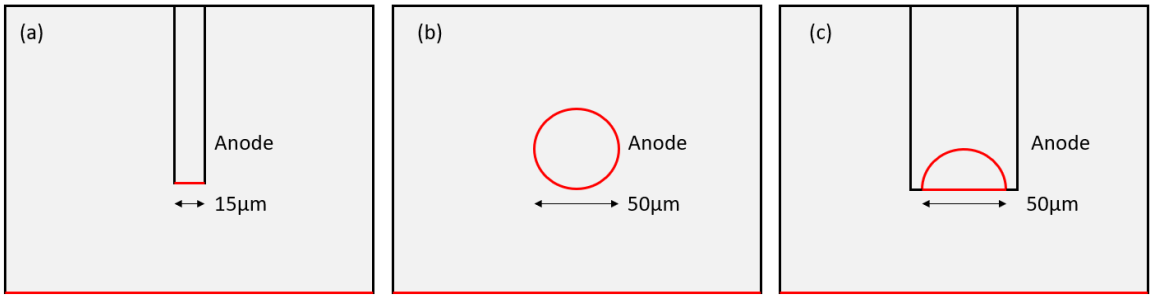

Fig. 3-9. Structures modelled in this work. Red lines are indicated by electrodes and are the anode and cathode. The three structures are (a) a traditional LECD wire with 15µm diameter anode, (b) a WLECD 50µm wire anode strung parallel to the cathode, and (c) a WLECD 50µm wire anode that is encased in an epoxy block and polished to expose the wire.

to the entirety of the anode as with the WLECD example in Fig. 3-9(b). All cathodes in Fig. 3-9 are displayed as the red line at the bottom. The cathodes are initially set to flat lines to represent a polished surface. Once growth begins, the preceding growth layer becomes the new cathode, which continues every 5μm until the desired growth height is achieved. Some of the simulations keep the anodes static in a single location above the cathode while others move the anode progressively farther away from the anode as performed in LECD studies. A mix of all scenarios was performed here to obtain a comprehensive analysis of each anode configuration.

The final aspect of model setup included forming the insulation of the bath. Since the focus of the model is on the growth on the cathode, it is important to ensure conservation of charge within the system. For these models, the edges of the bath in black of Fig. 3-9 have properties of zero charge i.e., the walls do not interact with the system. The program is set up so that a zero-charge boundary simultaneously acts as 1) an infinitely continuous extension of the medium that it borders and 2) a location where charge cannot accumulate or pass in or out of the system. This ensures the electric field does not interact with the barriers and does not necessarily need to intersect the barrier normally, so field lines do not accumulate or become denser on sharp corners of the zero charge regions. The second stipulation regards charge loss due to stray current. All motion of charge due to the presence of the electric potential at the anode passes through the cathode and remains in the system. Since the model only includes electrostatics equations for the electric field analysis, this property is less important. The edges of the epoxy coatings on the anodes were also given the zero-charge parameter. The reason being the epoxy/electrolyte interface could lead to

undesirable simulation effects and add extra variables for troubleshooting e.g., different shapes of the epoxy coating for LECD and WLECD making comparisons inconsistent.

3.3.4 Configuration of the Mesh and Measurements

FEM analysis requires the use of a mesh to approximate continuous problems. The denser the mesh, the higher the accuracy of the continuous solution. However, a denser mesh has a longer computation time since there are more nodal points to calculate solutions from. Ideally, a mesh grid would have infinite points in the mesh to perfectly represent the real system. This is unnecessary here, and dense meshes are typically only required in regions of interest e.g., near the anode or growth sites on the cathode. Fig. 3-10 shows a general example of how the mesh grids were set up for WLECD during the first growth cycle when the cathode is planar, and after some period of growth occurred. It is important to set the mesh density in regions of interest so the spacing between mesh points is smaller than the observed feature size, otherwise the features will not be rendered in the simulation. This approach is iterative, as feature sizes were only observed when the mesh was at the highest density, but when simulations were too long to reasonably perform. The result of this approach is an optimized mesh pattern for each process that varies in density across the simulation. A much larger plating tank could be simulated when mesh densities were lower in unimportant regions such as the top extremes of the tank, which were only included for observational purposes. The cathode surface and anode regions were set to be the highest mesh densities. A set number of mesh points on the surface of the anode and cathode was optimized, as well as the density decay rate of the mesh into the simulated tank. The result of the latter can be seen in Fig. 3-10(b) when the mesh is less dense above the anode than below the anode, due to the lower density decay rate towards the cathode

than towards the top of the tank. In this way, the region between the anode and cathode can maintain resolution requirements to obtain an accurate representation of the electric field. This is much more important when a growth is simulated than during the primary growth stage when the cathode is a plane. There was a negligible difference when using a less dense mesh for the first stage on the cathode, which explains the differences of the cathode mesh densities in Fig. 3-10.

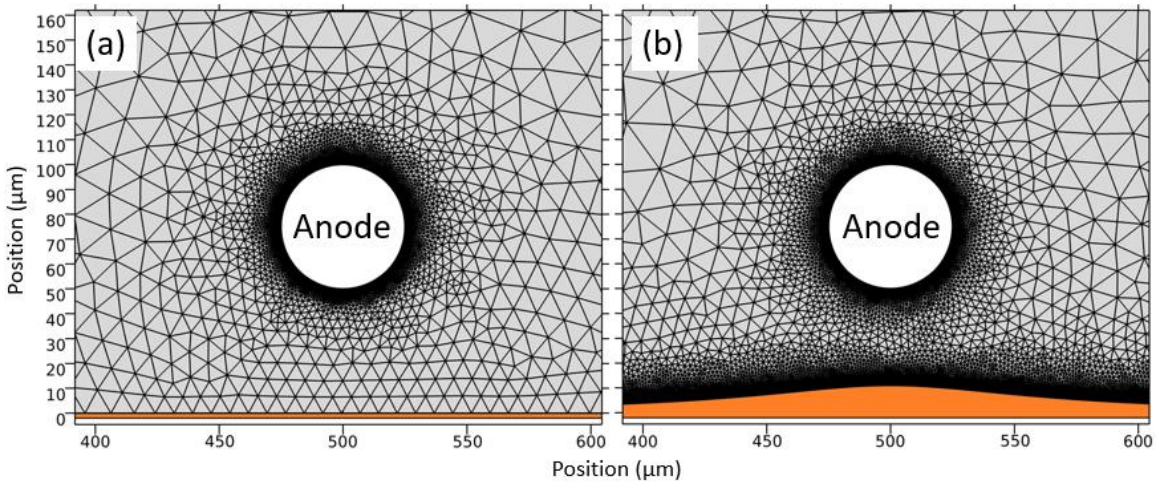

Fig. 3-10. Representations of the mesh for two electroplating simulations involving the WLECD wire anode. (a) is the mesh density on the first level of plating, when the cathode (orange) is flat and (b) is the much denser cathode mesh during a growth phase.

The mesh also plays a significant role in the simulation and measurement of the electric field. It was found that too dense of a mesh led to noise that became amplified over the growth cycles. Because of the limitations of the program, the growth curves were not continuous parametric curves, but a series of points spaced 200nm apart. If the mesh density ever exceeded the density of the points, issues would arise with growth completion. Fig. 3-11 portrays the mesh in clearer detail along with an explanation of a “false peak” problem. If the mesh density is set to one point every 200nm on the cathode surface, a solution is calculated at the actual point of the previous growth, and a clean continuous

solution is approximated to the next point. This next scenario examines when there is a single point added in between each actual point from the growth i.e., the mesh density is doubled over the entire surface of the cathode. The meshing software places a point on the curve between the two points that relate to the slope of the previous points. This is no different than doubling the number of points on the growth. However, since the meshing software is calculating the instantaneous slope from the previous points instead of using actual growth data, the points may lie slightly above or below where the actual value would be. This leads to either a slight peak or a valley on the mesh. On one growth cycle, this is not noticeable or does not affect the field outcome on a macro-scale. However, on five or more cycles, these peaks and valleys lead to high and low electric field points which accelerate or inhibit the growth in regions that would otherwise not see peaks and valleys. These false peaks become exacerbated with further growth cycles due to the positive feedback effect of the growth modelling. Small perturbations in the electric field become the next growth, which adds further perturbations to existing growths, etc. The only solution to mitigate the perturbations was to allow the mesh software to manipulate the geometry as little as possible, by using real data points as mesh points on the cathode. With this adjustment, final growths were significantly more uniform until high fields began to manipulate regions faster as the growth neared the anode.

The measurement of the electric field after the simulation was run needed to be in the region between the anode and the cathode. According to Gauss's Law, the net electric field does not exist inside the cathode, and due to the nature of the simulation, it does not exist on the infinitesimally thin surface. Thus, it must be measured outside of the cathode. Too close to the cathode and the measurements will read the field strength as approaching

infinite, but too far and an accurate value of the field strength will not be given. The measurement distance produced the same "false peak" issue when too close to the cathode, so it is important to discern the difference between high field measurements and false field spikes due to simulation limitations. The measurement curve, which is defined here as the list of points where the electric field was measured was chosen to be 1μm away from the surface of the cathode and remained constantly 1μm away as the growth continued towards

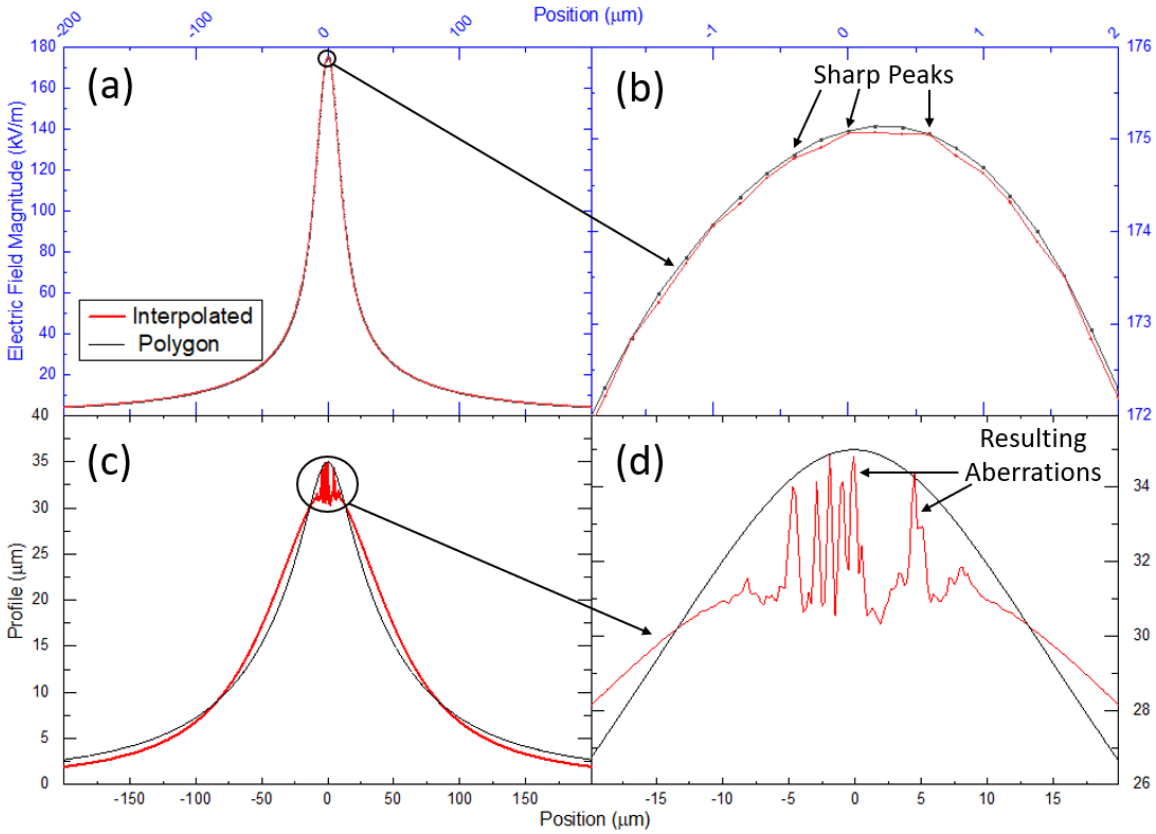

Fig. 3-11. (a)-(b) Measured electric field magnitudes for a polygon and software embedded interpolation function growth curve. The curves seem identical when first viewed in (a), but when the peak is viewed closer in (b), there are artifacts present (labelled sharp peaks) that contribute to false electric field growth. (c)-(d) Resulting profiles from a 35μm growth curve using the polygon and interpolated curves. The interpolated curves in (d) show significant deformations of the growth curve. At the high fields present during LECD, these artifacts become quite significant over several growth iterations.

the anode. The measurement curve matched the shape of the growth exactly, minus the fact that it was 1µm closer to the anode. The 1µm distance was chosen empirically. Erratic field lines that were considered noise were quelled at measurement distances exceeding 500nm from the cathode, so 1µm would act as an additional buffer from the noise. Also, the 1µm measurement curve was much less than the growth increments of 5µm, so it was sufficiently close to the cathode for the accuracy of the modelled growth. Fig. 3-12 shows the measurement curve above a growth.

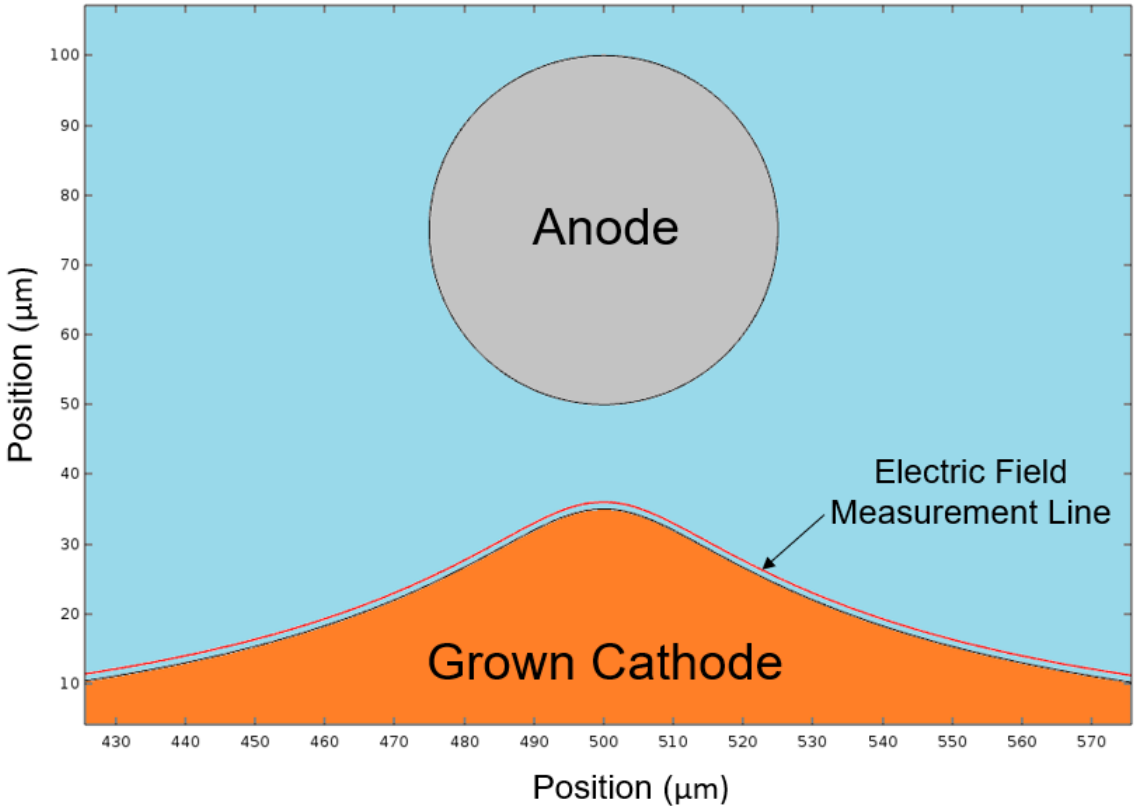

Fig. 3-12. Electroplating simulation showing where the electric field magnitude is calculated relative to the cathode. Measurement line is adjusted to 1µm above the cathode after every growth period.

3.3.5 Electric Field Growth Model using FEM

The growth process involved several repeating steps to achieve the desired structure height. The first step of the growth process involved applying an electric potential to the anode under observation and measuring the electric field over the planar cathode at the measurement curve, which was 1μm away and parallel to the cathode. Next, the electric field magnitude across the measurement curve was converted to units of length by a normalization equation shown here:

$$\{\text{Growth Profile}\} = \frac{\{\text{Electric Field Profile}\}}{|\text{E}|_{\text{Max}}} * 5\mu\text{m} \quad (1)$$

where {Growth Profile} is the list of points making up the curve of the next growth curve, {Electric Field Profile} is the list of points of the electric field of the current simulation measured on the measurement curve, $|E_{Max}|$ is the maximum electric field value found in the list of the {Electric Field Profile}, and 5μm is the growth step chosen in this work.

The normalized growth profile found using the Equation 1 is added to the height of the cathode, forming a simulated plated growth 5μm tall. These steps are repeated, but with the next 5μm calculated growth profile being added to the previously summed growth profiles instead of just the planar cathode height. Fig. 3-13 demonstrates the general steps involved.

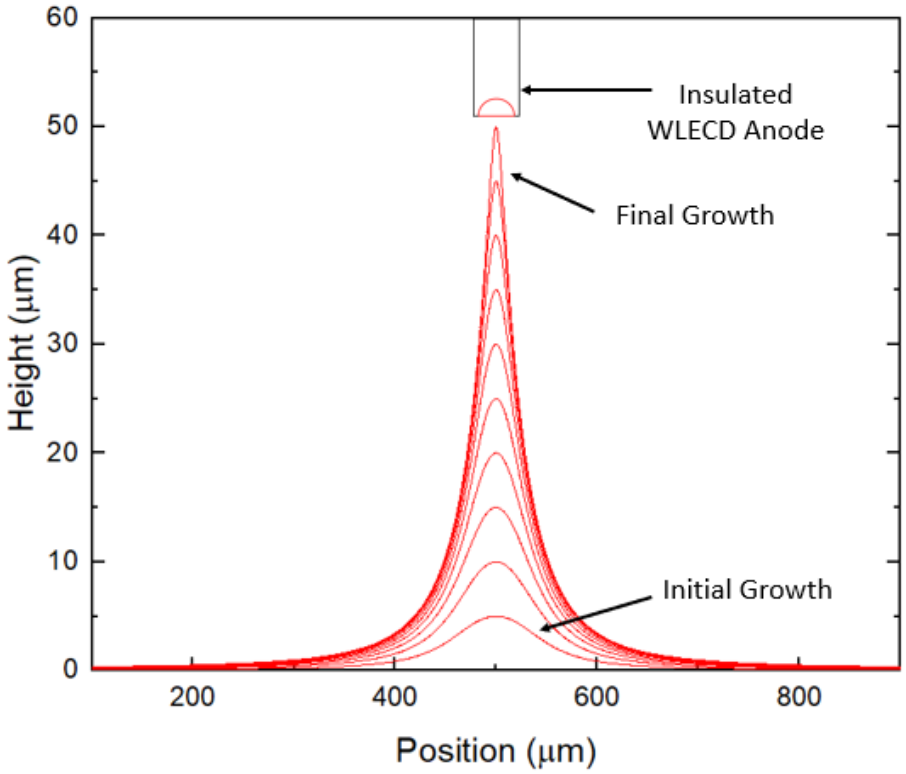

Fig. 3-13. Plot showing the 5µm growth steps for a full 50µm tall growth using the 50µm WLECD insulated anode set 50µm away from the cathode. The WLECD anode is to scale in the x-direction.

With the general model established, the parameters need to be set and the model verified using empirical data. The electric potential, anode sizes, and electrical permittivity of the bath remained constant through the work, but the growth height, anode/cathode spacing, and anode movement were varied. The electric potential was set to 2.4V and the anode sizes were set according to Fig. 3-9 for each localized plating process. To verify the model, a model was created to compare a WLECD structure with the following parameters in Table 3-2. As it is shown, the model parameters were set as close to the actual values as possible, except for the surface roughness. The model was grown to 5µm, 10µm, and then 11µm in 3 total stages. Fig. 3-14 shows the growth profile of the simulation with the range of profiles collected along the plated WLECD line. Physical profiles were generated by a

Table 3-2. WLECD growth model parameters comparison to actual WLECD parameters.

Parameter	WLECD Simulation	WLECD Actual Growth
Electric Potential (V)	2.4	2.4
Anode/Cathode Initial spacing (μm)	50	50
Anode Movement	NO	NO
Final Growth Height (μm)	11	11
Bath Permittivity (V/m)	1.0	Unknown
Cathode Surface Roughness (Ra)	0	>8.00

Dektak profilometer. On the line that was plated using WLECD, the profilometer was scanned every 1mm for 5mm and the resulting profile max/min values were recorded and displayed with the modelled profile in Fig. 3-14(a). The results matched well with the modelled profile, and so work continued with this growth method.

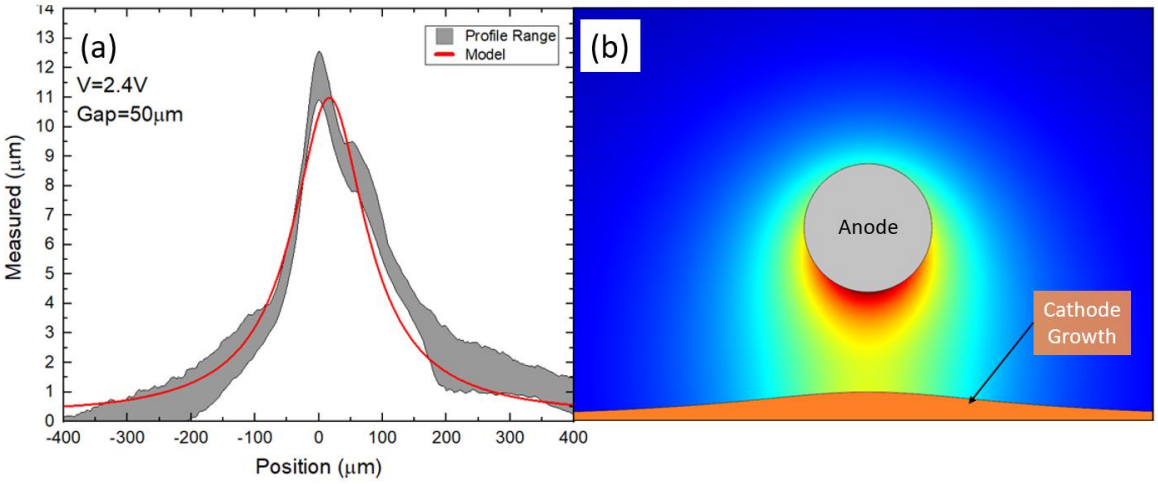

Fig. 3-14. (a) Simulated growth in red and measured value range of profile cross sections for WLECD. (b) Simulation physical setup with rainbow coloring representing the electric field magnitude. The cathode in (b) has grown to the red curve in (a).

3.3.6 Effects of Geometry on Growth

A large range of anode/cathode spacing values were tested, from 10μm to 50μm to showcase the differences between each localized plating technology. The profile shapes differed for each technology, so a method of comparison needed to be established. When electroplated, the rounded WLECD anode produced profiles with a sharp peak and a wide base, while the LECD anodes in literature produce a more columnar, rectangular cross section.

The results from the plated line simulations are shown in Fig. 3-15. Fig. 3-15 shows the growth profiles for different initial gaps for each anode. Despite being close to the anode on small initial gaps, the rounded WLECD anode in Fig. 3-15(a) still produces a curved profile with little to no rectangular features desirable for solar. This profile was seen in all measured data when electroplating using the WLECD technique. The LECD anode in Fig. 3-15(c) also shows this same profile trend, although since the LECD anode is only 15um in diameter, the profiles are narrower than the WLECD wire anode in Fig. 3-15(a). The insulated 50um WLECD anode in Fig. 3-15(b) displayed very rectangular shaped growths until the anode exceed approximately 30um. Past this point, the curved growth profile of Fig. 3-15(a), (c) returned. For LECD techniques, it seems the flat profile of the insulated and sanded WLECD wires works best to produce a more rectangular profile for solar. However, this rectangular profile was not seen in the LECD anode. It is important to note that for every anode, the profiles began to resemble each other after some large anode/cathode spacing. Past a certain distance, all anodes begin to resemble the same shape i.e., points. This is intuitive since this is the basis for many approximations in electrostatics. While the insulated WLECD wire and the LECD wire had the same shape, the latter was

one-third the size of the former. So, a 10um anode cathode gap is 67% of the LECD anode diameter while a 10um gap is only 20% of WLECD wire anode diameter. The smaller LECD anode needs to be much closer to create more rectangular profiles. This has an interesting application for solar and mass production. The anode/cathode spacings in this work are on a very small scale and may be difficult to consistently achieve in a mass-production environment. But, if solar applications required 70um Cu fingers for a shingled cell as was modelled in Section 3.1, or 200um wide Cu busbars, the anode/cathode spacing would scale with the size requirement i.e., a 200um busbar would not need to be plated 10um away from the anode, but maybe 100um, with more room for error as the size increases. This is a much more manageable anode/cathode gap to maintain. Regardless, it is clear from Fig. 3-15(a), a rounded profile, and thus a point anode, is not good for rectangularity. Future work with WLECD for solar should utilize a flatter anode to electroplate a desirable rectangular cross section on a finger.

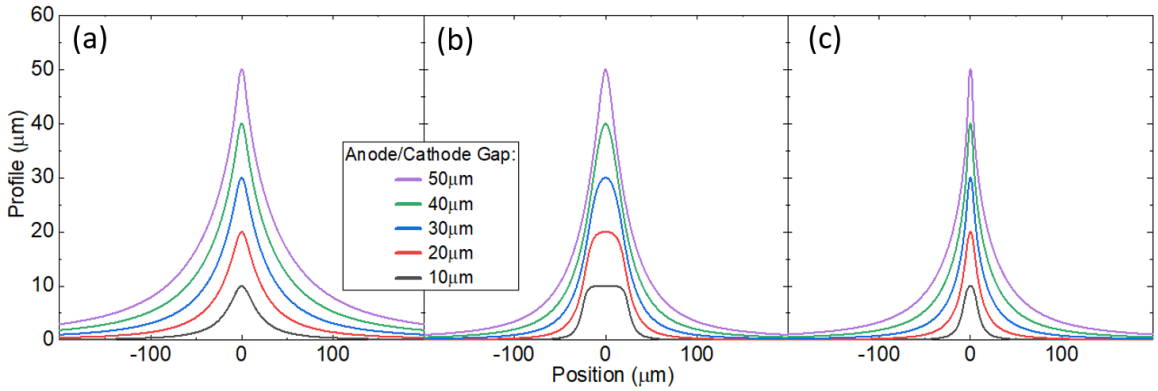

Fig. 3-15. 10-50μm profile growths for the (a) bare 50μm diameter WLECD round anode, (b) insulated 50μm diameter WLECD anode, and (c) insulated 15μm diameter LECD anode. Each curve represents an entire growth cycle at the specified anode/cathode gap. The anode was also static for each growth i.e., the anode was placed in the described anode/cathode gap and remained for the entirety of the simulated event.

3.4 EFFECTS OF ANODE COMPOSITION ON LOCALIZED PLATING

LECD anodes have been reported exclusively composed of more noble metals such as Pt, which can be used in a variety of plating chemistries as an inert anode [68]. Anode composition, whether Pt or Cu, engage different electrochemical processes and are summarized in Fig. 3-16. Inert anodes such as Pt are insoluble in Cu sulfate solution, and thus, the geometry of the micro-anode remains constant throughout the plating session, with the added benefit being it does not need to be replaced. Jansson et al demonstrated the epoxy sheathing insulating the Pt anode tip may fray over time, which does affect plating, but the Pt anode itself remains intact [71]. Additionally, the electric field remains constant under the anode at a particular distance, making deposition rates and other parameters consistent and controllable. Since Pt is inert in solution and isn't reduced, another electrochemical reaction must take place for Cu ions in the electrolyte to plate to the cathode. The Pt reaction operates at a higher electric potential which hydrolyzes water and liberates oxygen at the tip of the micro-anode. The oxygen can "stick" to the micro-anode due to the surface tension of water and interfere with LECD plated structures [84]. Workarounds have been given in literature, but the phenomenon is ever present when using inert anodes [84]. Conversely, the Cu anode depletes in solution as the Cu anode reaction with sulfate ions dissolve Cu into the bath. For LECD and WLECD, this can cause 1) geometry alterations throughout the course of plating, affecting the localized electric field crucial for LECD and 2) disintegration of the anode wires, necessitating anode replacement. However, Cu anodes do not generate oxygen near the half-cell potential. Additionally, the placement of the Cu anode in the LECD work area may reduce depletion

of Cu ions necessary for higher fidelity plating. To assess the effects of each anode type, both Pt and Cu wires were used as anodes for WLECD.

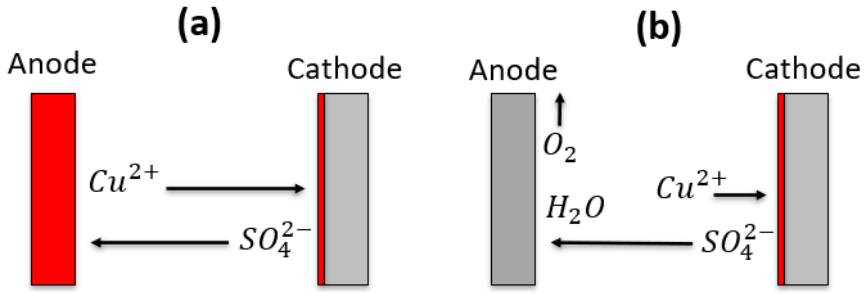

Fig. 3-16. Simplified electrochemical process diagrams involving a (a) Cu and (b) Pt anode [85].

3.5 LOCALIZED ELECTROCHEMICAL DEPOSITION USING LARGE AREA CU ANODE

Several iterations of LECD Cu electroplating were performed with the large area anodes. In addition to the full area H-bar pattern, contact pads and different line width patterns were implemented. In Fig. 3-17, a TLM and line width structure used in Section 2.3.4 and 2.3.5 was exposed onto the photoresist on the large area Cu anode. A 125mm

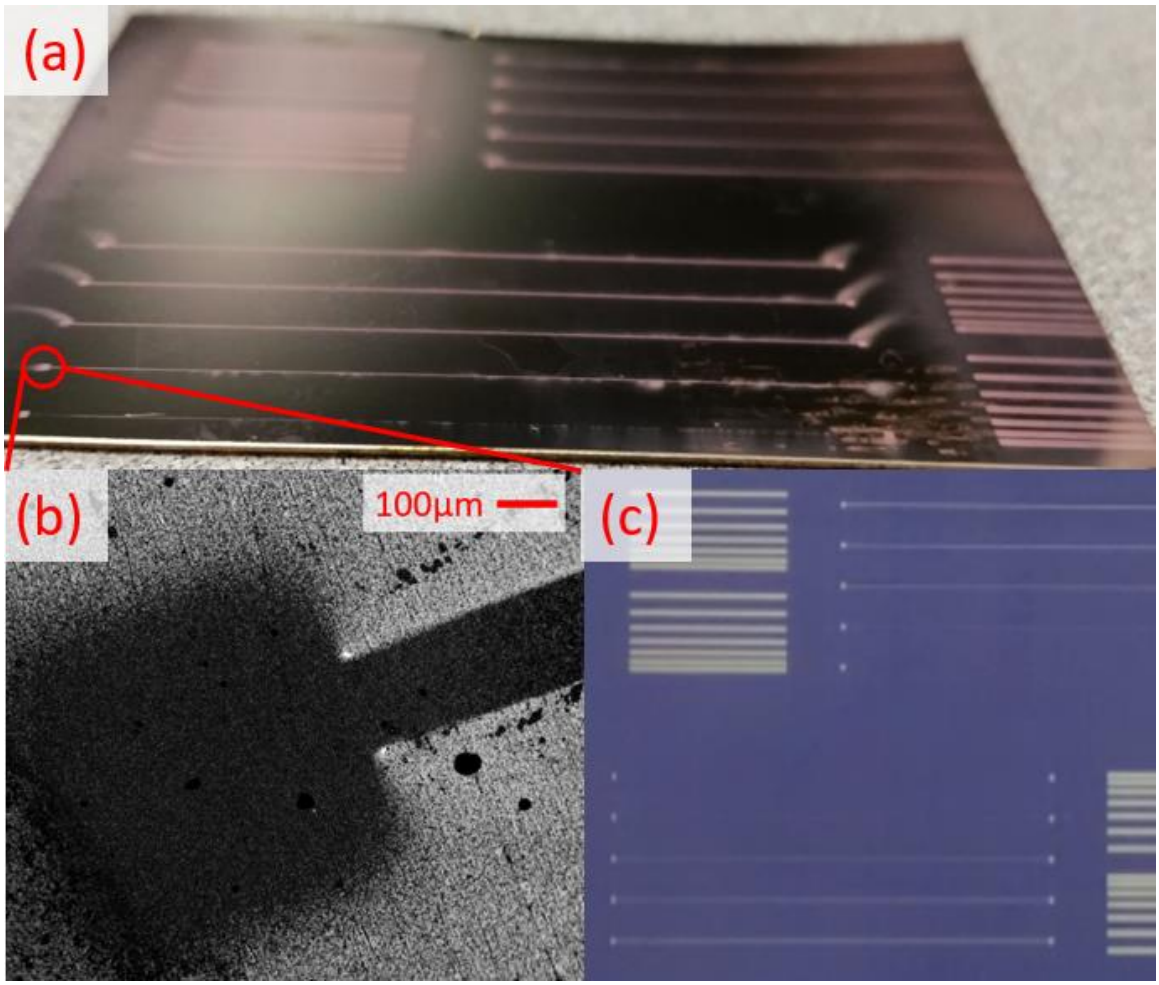

Fig. 3-17. One masking method of the large area anode to determine the ability of this LECD method to imprint an image onto a brass substrate. The (a) brass substrate with a (c) TLM and line width pattern previously used in this work from measuring contact and line resistance. (b) A close-up image of one of the square contact pads at the end of one of the lines. Besides the photoresist mask on the anode, no other mask was used on the brass plate. Wisps at the end of the lines in (a) are due to ghost plating.

silicon solar cell was also plated with a front grid pattern onto ITO with an Ag seed layer. There was some difficulty contacting the wafer, unlike the brass substrate which could be back contacted, so results were inconsistent. However, some fingers were well defined and are shown in Fig. 3-18. For all electroplated results using the LECD large area anode, granular Cu deposits and electroplating cessation in some regions on the cathodes could be

attributed carrier depletion, if the delaminated photoresist blocked the channel openings, anode polarization or other factors. This is discussed in more detail in Section 3.7.

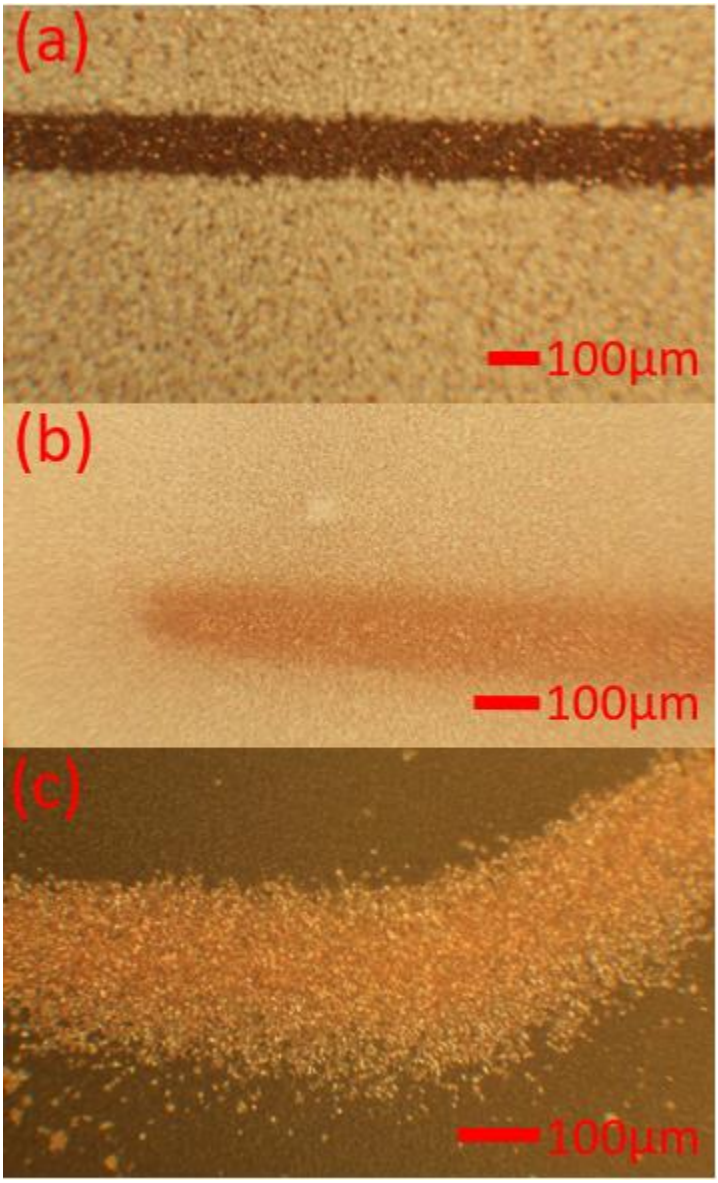

Fig. 3-18. Optical microscope images of (a) a Cu finger and (b) the end of a Cu finger prior etching of the Ag seed layer and (c) an older style perimeter finger set at the angle of the solar cell diagonal cut after Ag etching. Cu formed is granular in nature due to the fast plating rates, and darker colors such as what is seen in (a) can be seen if granules are large creating a rough surface texture.

The Cu anode dissolved at a faster rate than anticipated during a single plating cycle, leading to greater uncertainties in electric field strength and general shape, which translate to uncertainties in Cu structure shape on the cathode. Also, when Cu was removed from between the photoresist channels, the anode began to dissolve laterally underneath the photoresist, leading to the delamination of the photoresist causing possible obstructions of the plating site on the cathode. Fig. 3-19(a) demonstrates this phenomenon. This is reinforced by the optical images of the anode taken after the photoresist mask was stripped off in Fig. 3-19(b), (c). The pitting seen in Fig. 3-19(b), (c) was much larger than the measured photoresist openings prior to electroplating. The red outlines display the

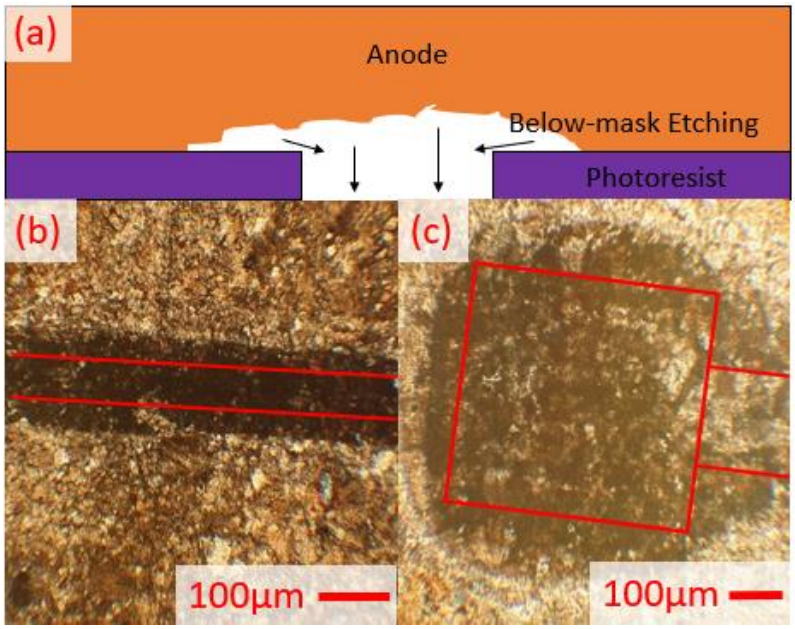

Fig. 3-19. Optical microscope image of depleted Cu anode in different regions. Red lines show approximate location of photoresist mask openings. Clear undercutting of the photoresist can be seen which led to loss of adhesion and unpredictable plating.

approximate sized photoresist openings for each pattern. Since the photoresist chemical stripper does not etch Cu, the only way the pitting could have formed was during electroplating. Due to these factors, LECD on this scale must be performed with a non-

consumable anode to retain fidelity of the plated surface across the wafer to provide repeatable results.

3.6 WLECD WITH INERT PLATINUM ANODES

The first WLECD structures to be examined are those plated using Pt as the anode. Circulation of solution via pump was required to prevent oxygen buildup near the plating regions. When circulation was performed, plated lines such as the ones shown in Fig. 3-20 provided clear results. The images in Fig. 3-20 were taken from different samples under different electric field conditions, illustrating the viability of the tensioned wire process to create clearly defined plated lines. The two plated lines occurred with different anode/cathode spacings, and a wider and smoother profile is formed in Fig. 3-20(b) by moving the anode farther away from the cathode. However, Fig. 3-20 primarily showcases the uniformity of the lines plated using WLECD.

Profiles taken of several plated lines compare the effect of electric field conditions on the resulting profiles, as well as uniformity along the line. Changing the electric field via voltage and anode/cathode plating gap is similar to cross sectional results from previous LECD literature e.g., the increase in voltage in Fig. 3-21(a) narrows the profile of the LECD plated cross section. Numerous sources have shown via simulations and empirically, this is the effect of ions in solution being drawn to the high electric fields; increasing the voltage increases preferential plating in regions of high electric field, such as under the anodes [74], [86]. Additionally, the same voltage will have different electric fields at different anode gaps, which corresponds to different plating rates near the anode. Fig. 3-21(b) shows that changing the spacing alters the plated cross-sectional profile. Larger gaps lower the electric field and create a smaller but more homogeneous plated structure

along the anode wire. The result is a smoother and more rounded profile. Smaller gaps create higher electric fields which accentuates imperfections in the anode wire. Traditional LECD uses polished anode tips with precision flatness to guide deposition. This flatness along the anode wire was difficult to control using a tensioned wire and not achieved in this work. Rounded wire cross sections, stretching of and kinks in the wires, and sharp corners generate different plating current densities for the same voltages along different lengths of the wire. Thus, the average height profile of the plated lines in Fig. 3-21(b) become more erratic, with multiple sharp peaks and less line uniformity when the anode/cathode gap is decreased. Due to the resolution of physical profilometry which was used to measure the peaks in Fig. 3-21, some peaks or heights may not show in the profile i.e., the sharp peaks in Fig. 3-21(b) may be taller, or there may be more than what is shown in the plot.

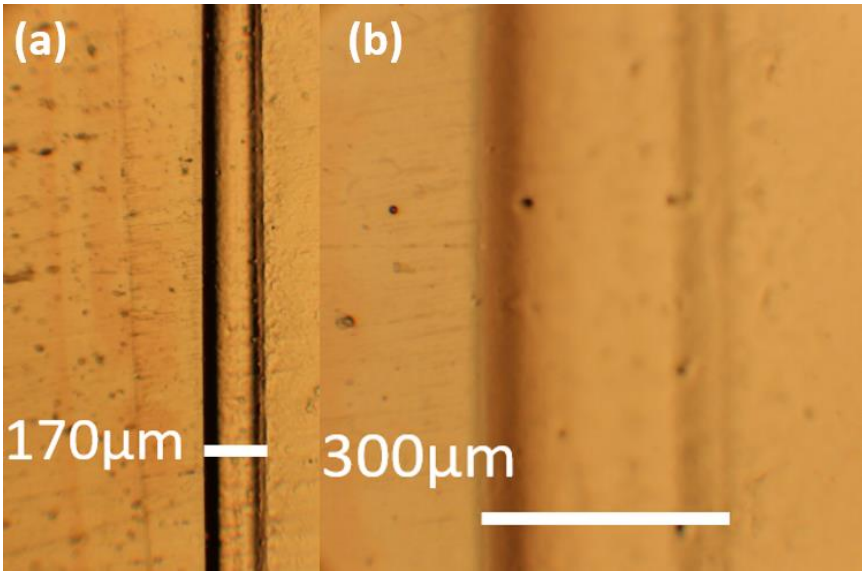

Fig. 3-20. Optical microscope images of Cu lines deposited on different brass cathodes at 2.3V with (a) 40um spacing and (b) 60um spacing between the anode and cathode. Optical measurements were taken using a calibrated microscope. Uniformity of these line cross sections were maintained around 4mm.

Line uniformity of locally plated lines were examined at different points along the length of the line. Physical profilometry scans were performed on a sample every 1mm for 4mm and is shown in Fig. 3-21(c). It is important to note the x-axis is the scan length and not the line width. The samples were set by hand, and slight changes in sample orientation could lead to slight line width variations, on the order of tens of microns. The profilometry scans show for this sample, average line height is consistent along 4mm of the active area of the line. While deviations are expected, no major deviation occurred that compromised the plated line cross section e.g., breakages.

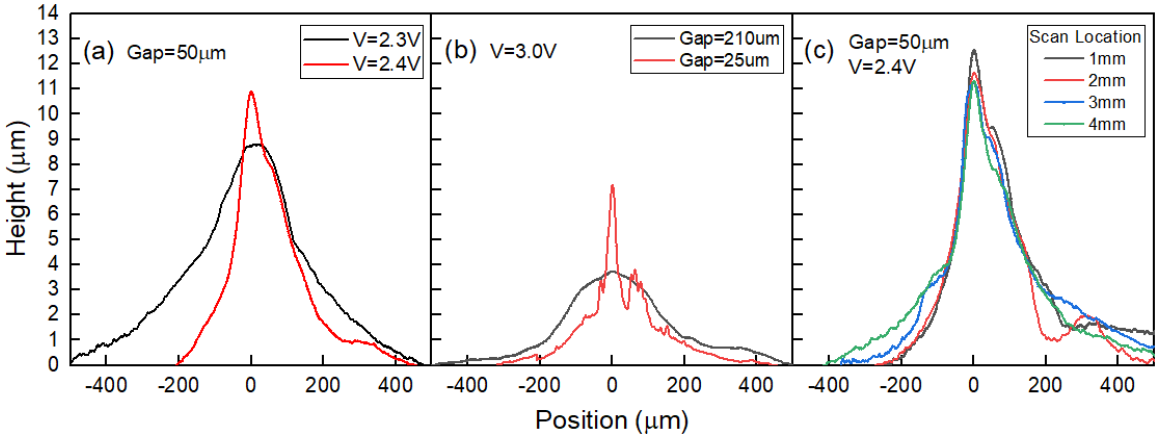

Fig. 3-21. Physical profilometry scans of plated samples. Plots showing (a) effect of voltage on plated cross section, (b) effect of anode/cathode gap, and (c) consistency of line cross-sections along 4mm of plated line. (a) and (b) show averaged heights in several locations along their respective sample line.

The samples were examined continuously using an optical microscope along the length of the entire line scanned by the profilometer. Over the 1cm active area of plating, it was typical to find 4mm of consistent plating profiles for many samples. The flatness and anode surface parallel seen in traditional LECD were not as pronounced in this work, due to the two-dimensional presence of the anode over the cathode, but uniformity was still achieved. However, it is predicted over larger line lengths e.g., >100mm for PV metallization lines,

it will be more difficult to achieve line uniformity. For these industrial applications, flatness and parallel will become an issue, especially with the possibility of multiple lines being plated in parallel.

In areas outside the consistent line uniformity, line breakages, underplating and overplating were some of the issues encountered. These may be predominantly attributed to wire resistance and electric field variations along the anode wire. For the former, since the anode wires were electrically contacted at the ends, resistance of the Pt wire led to lower plating densities near the center of the samples. This is shown as a slight tapering of the line width across the sample. The scale of the tapering occurred at millimeter distances and the taper itself could change the line width by 100um, so it was difficult to procure an image to depict this. For the latter case, anode/cathode gap differences and wire kinks led to high- and low-density plated areas, which was imaged in Fig. 3-22. Fig. 3-22 depicts non-uniformities possibly caused by kinks, leading to stray electric fields and overplating outside the line. Finally, a sharper peak can be seen on the bottom part of the line compared to the top in Fig. 3-22.

As previously indicated, oxygen was liberated during all plating cycles involving the Pt anode. When the solution was not circulated, oxygen accumulated near the anode wires. In traditional LECD work, the cathode is typically placed in the bottom of the bath and the anode is a single point above the surface. For this setup, the cathode lay above the anode wire which led to the trapping of oxygen around the anode wire. It was observed that lower plating currents produced small bubble sites and higher currents produced large bubble sites as those seen in Fig. 3-23. This is expected since the formation of oxygen is directly correlated with the amount of Cu being plated. In addition, more anode surface area is

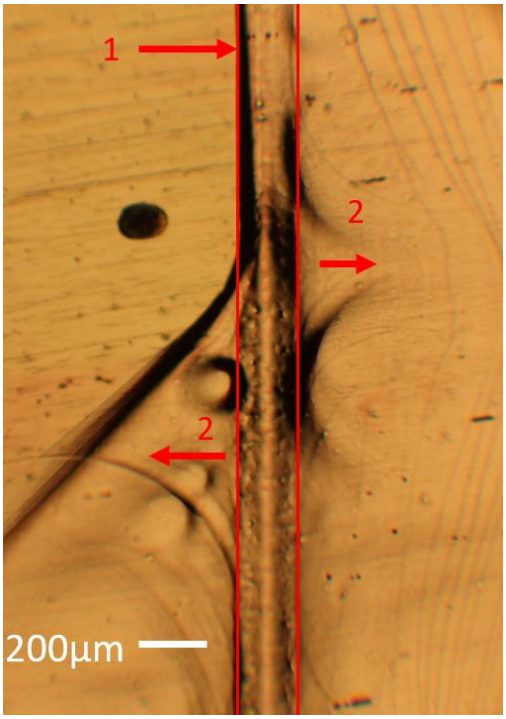

Fig. 3-22. Plated line outlined by (1) on a brass cathode. Deviations in the line formation occur at (2) and are a result of overplating in those regions.

exposed on a bare wire compared to an epoxy/glass sheathed anode used in LECD, leading to more oxygen formation sites. The experiments in this work that did not circulate solution are shown in Fig. 3-23 and resulted in lines difficult to interpret. While this effect does occur with traditional LECD, the effect is exaggerated here, where the large channel between the spacers traps the oxygen and inhibits plating along the channel. Coating the platinum anodes with an epoxy or other insulative coating and exposing the single face of the anode toward the cathode could help mitigate the issues with tensioned wire LECD. Reducing the exposed surface area of the Pt wire reduces oxygen generation sites and therefore reduces the rate at which bubbles form near the anode. Coatings on the back and sides of the wires reduces the stray electric fields that can lead to unwanted outward plating. The coating could also strengthen the wires and reduce the effects of wire imperfections

such as notches or kinks, which may cause the detrimental effect of stray electric fields. Merely using a bare Pt anode in this work is effective for producing lines, but tensioned anode LECD could be greatly improved with more control over the listed problems above using a coating.

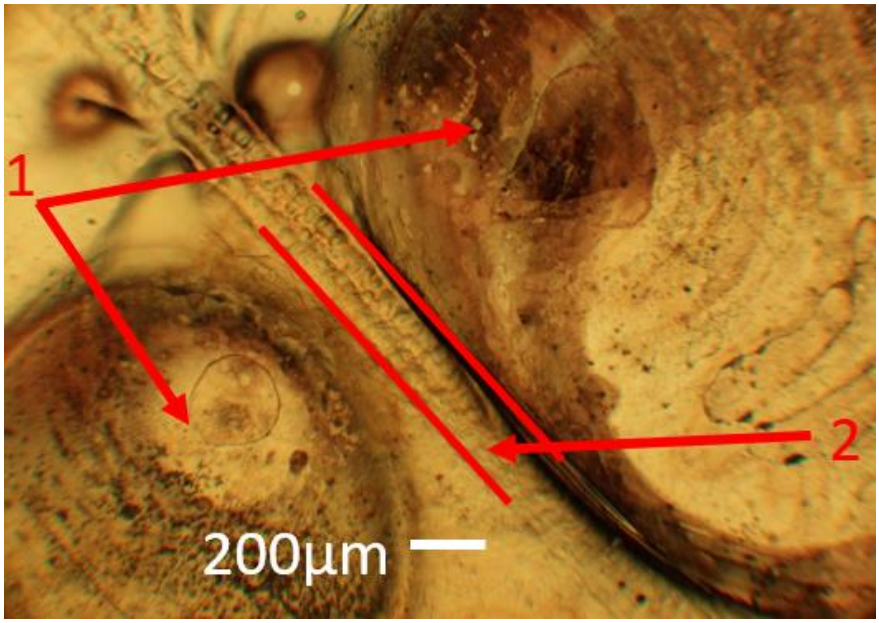

Fig. 3-23. Optical microscope image of Cu line deposited on a brass cathode. Evidence of bubbles formed during plating manifest as (1) circular regions lacking deposited Cu. The (2) plated line is still visible despite inhibited growth due to oxygen buildup. Bubble sizes are dependent on plating voltage and location along the anode wire.

3.7 WLECD WITH CONSUMABLE CU ANODES

The resulting lines plated using the 76um Cu anode wires were inconsistent and difficult to distinguish from background brass due to extremely short plating time. Voltages above the half-cell potential resulted in plating currents dissolving the anode in certain regions in seconds. The wire anode broke under tension as areas dissolved and the plating session was ceased. For these experiments, the only consistent growths were the dark plated regions shown in Fig. 3-24. These appear to be dendritic growths, columnar in nature, and were

measured to be >50μm in height. Other regions along the line contained little to no plating. It is predicted that imperfections in the Cu wire such as bends, led to preferential plating in these regions. This is expected, but the high current density at the half-cell potential exacerbated these effects, leading to a series of columnar growths in specific regions under the Cu anode wire. This is supported by breaking of the wire in a single region, as well as the presence of dendrites on the plated columns. Wire breakage, contrasted with complete dissolution of the wire, is caused by preferential plating of the anode at a single point. Larger electric fields due to kinks or bends drive higher plating current densities in these regions, which dissolve points on the anode wire faster than in other locations, whereas a uniform anode would dissolve equally in all locations. Dendrites could be formed due to depletion of bath additives caused by large ion migration in the bath, or depletion of Cu ions near the cathode. Both result from applying higher current densities the bath is capable of sustaining.

Due to the limited supply of Cu in the thin anode wires used for this work, as well as the high current densities at the half-cell potential, growth would occur faster in regions under anode imperfections. The relatively quick dissolution rate of the anode wire would lead to a positive-feedback effect, portrayed in Fig. 3-24(b), where plating rates would increase as column grew taller and the anode/cathode spacing decreased. Since the plating current is fixed for a particular bath chemistry near the half-cell potential of a Cu anode, possible solutions to this problem are to increase the diameter of the anode wire or increase the spacing between the anode wire and the cathode, reducing the current density. This would provide more Cu ions in solution and increase the localized surface area on the

cathode for plating respectively, decreasing overall current density to reduce dendritic growth.

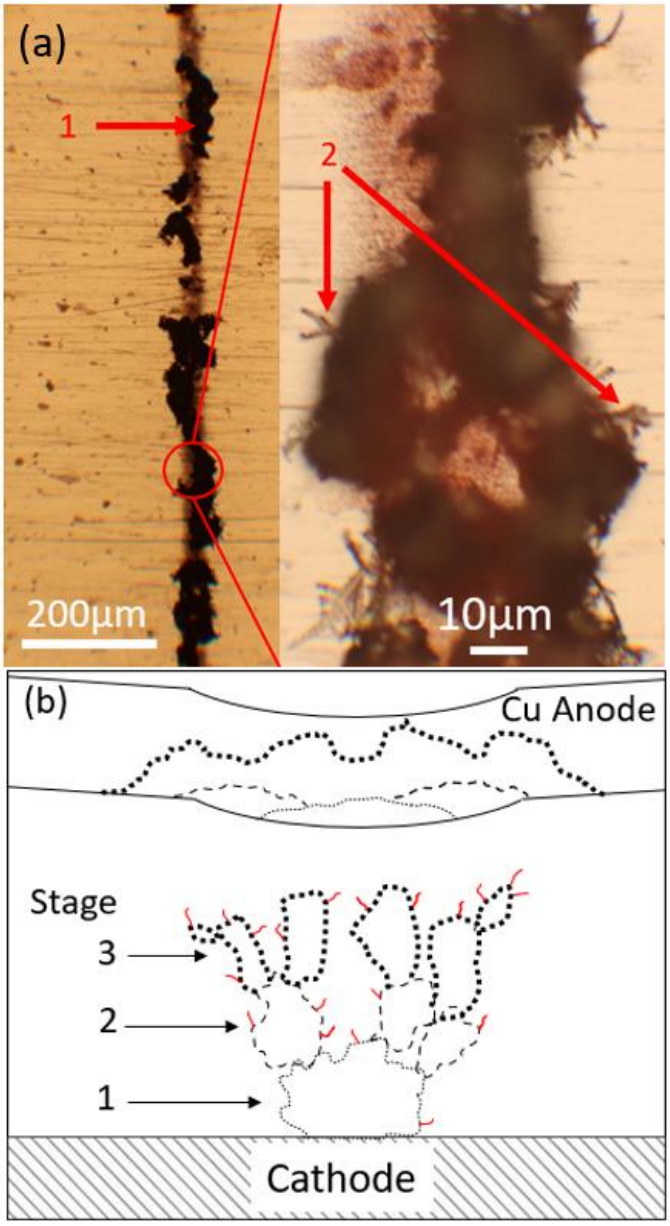

Fig. 3-24. (a) Images of Cu deposited above the half-cell potential. Plating occurred quickly in certain regions which led to (1) pillared/clumped growth and (2) Cu dendrites on many levels of the pillars. (b) Vertical cross-sectional diagram showing 3 stages of growth and Cu anode dissolution; initial imperfections such as a bend shown here in a Cu anode under high current densities could lead to a localized column-like growth that can break the anode. Dendrites (red) would occur in many places where growth began but was outpaced elsewhere on the columns.

Due to the issues listed above, plating was also performed with Cu anode wires below the half-cell potential, with the goal being lower current densities. This did produce clear deposits of Cu under the anode, but the deposit was granular and had extremely low surface adhesion as seen in Fig. 3-25. In extreme cases, adhesion was so poor the deposits could be removed with rinsing. Also, plating ceased after about 1um of deposited height. It may be the plated Cu ions did not have enough energy to properly adsorb to the substrate, or the anode or cathode was becoming polarized. It might be possible to utilize this deposit as a potential seed layer, but the adhesion must be greater, and the Cu deposits electrically active with the substrate. This could be achieved in a post-plating step such as sintering. Without this post step, plating below the half-cell potential results in deposits that would not be classified as a plated structure, regardless of line consistency and other metrics used in this work.

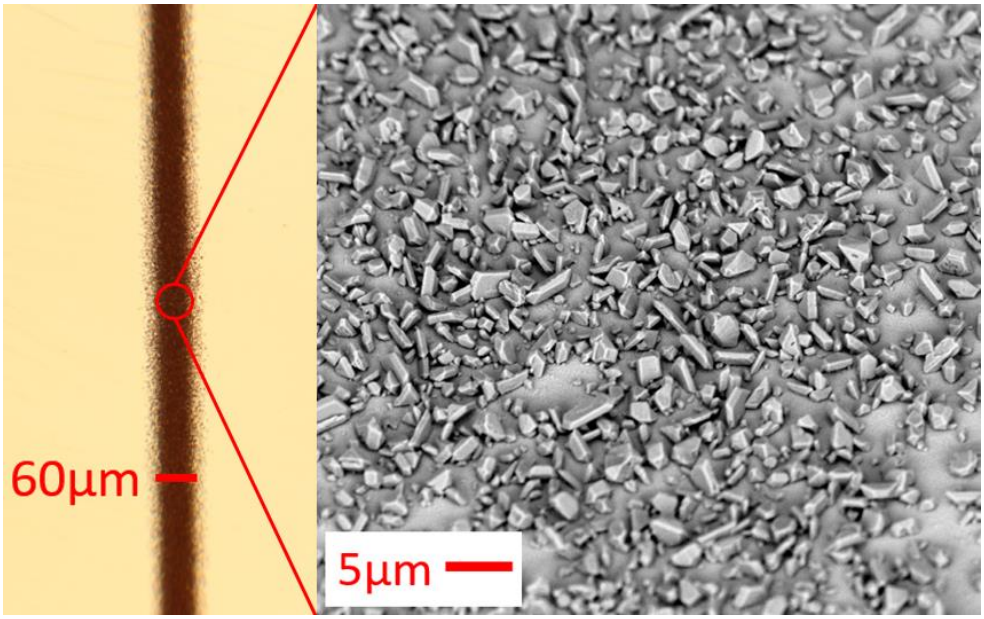

Fig. 3-25. Images of Cu deposited below the half-cell potential at 70mV with an anode/cathode spacing of 30µm. Plating occurred on a silver seed layer on polished silicon. The rough surface of the copper granules on the left gives the appearance of a darker line when observed with an optical microscope.

CONCLUSION

In conclusion, all patterning methods attempted in this work could achieve resolution close to 60μm, which was sufficient to increase the efficiency of the Ag printed SHJ cell by 0.5-1% absolute. All photoresists could produce the required finger thickness, however, the fingers plated using shorter resists would “mushroom” to add to shading losses. PVD Ag seed achieved the lowest specific contact resistivity and the best adhesion. It was found that stripping metal oxides for PVD Ni was critical to improve adhesion and contact resistance. It was not possible in this work to optimize light induced plated Ni to achieve a good adhesion to the sputtered ITO. Physical and electrical resistance tests were performed for each seed layer to compare them. Unfortunately, no seed layer fared similar in characteristics to the PVD Ag this work. As such, completely removing Ag was not possible from this production process, but at least the SHJ cells produced with a PVD Ag seed layer consumed 100x less Ag than a fully Ag screen-printed grid.

The LECD process showed promising results for mask-less electroplating method. For Cu anodes, lines of 180um were achieved with a patterned anode that had an initial mask opening of 60-70um and an initial plating distance of 20um. Considering the changing field due to dissolution of the anode severely impacts plating quality and lateral plating resolution, the author predicts much better plating quality from a compliant and non-depletable masked anode source in future work.

Mask-free plating techniques such as LECD contain great potential for the semiconductor industry. However, LECD plating scope thus far being limited to high-aspect ratio pillars fails to provide a feasible application in this industry. The WLECD process was developed in this work and presented for the first time as an LECD method of

depositing lines. Up to 4mm of continuous lines have been formed in this setup, with little deviation in cross sectional geometry, using tensioned anode wires of Pt and Cu to different effects. Cu anode wires provided very good control, but only when electroplating below the half-cell potential of the reaction. This created very uniform and controllable lines, but the lines were of poor quality and did not adhere to the substrate. It is possible for future work this layer could be sintered with the substrate to provide a seed layer for further plating. The Pt anode wires were effective in producing legitimate lines as deposited with no further processing steps compared to the Cu anode wire. However, oxygen formation in the setup attempted here remained under the substrate and was difficult to remove without high volume pumping of solution. This pumping may have moved the anode wire to a degree that would cause stray plating. Issues presented in this work regarding line formation are related solely to non-idealities in the setup proposed here, and are not limitations in the WLECD process itself. Errors in wire formation and tensioning, length of setup, and use of insulating coatings can all be optimized to produce electroplated lines of any size and quantity. Additionally, the WLECD setup proposed here can be modified to place anode wires in parallel or perpendicular, allowing for simultaneous plating of an entire grid, such as ones seen on the front of solar cells. Thus, this work presents a first step for true mask-free plating applications requiring lines on a substrate.

Additionally, modelling showed that a polished rectangular LECD anode provided superior squareness of electroplated profiles compared to a round wire. Therefore, it was decided that a polished and encased anode would be the next step to providing more control over the electroplated lines using Pt anodes.

REFERENCES

[1] K. Okuda, H. Okamoto and Y. Hamakawa, "Amorphous Si/Polycrystalline Si Stacked Solar Cell Having More than 12% Conversion Efficiency," *Japanese Journal of Applied Physics,* vol. 22, no. 9, pp. 605-607, September 1983.

[2] M. Tanaka, M. Taguchi, T. Matsuyama, T. Sawada, S. Tsuda, S. Nakano, H. Hanafusa and Y. Kuwano, "Development of New a-Si/c-Si Heterojunction Solar Cells: ACJ-HIT (Artificially Constructed Junction-Heterojunction with Intrinsic Thin-Layer)," *Japanese Journal of Applied Physics,* vol. 31, pp. 3518-3522, September 1992.

[3] M. Green, Y. Hishikawa, W. Warta, E. Dunlop, D. Levi, J. Hohl-Ebinger and A. Ho-Baillie, "Solar Cell Efficiency Tables," *Progress in Photovoltaics: Research and Applications,* vol. 25, no. 7, pp. 668-676, June 2017.

[4] "Panasonic HIT® Solar Cell Achieves World's Highest Energy Conversion Efficiency of 25.6% at Research Level," Panasonic Group, 10 April 2014. [Online]. Available: https://news.panasonic.com/global/press/en140410-4.

[5] "LONGi once again sets new world record for HJT solar cell efficiency," LONGi, 24 June 2022. [Online]. Available: https://www.longi.com/en/news/new-hjt-world-record/.

[6] "International Technology Roadmap for Photovoltaics (ITRPV)," 2020.

[7] D. Adachi, J. L. Hernandez and K. Yamamoto, "Impact of carrier recombination on fill factor for large area heterojunction crystalline silicon solar cell with 25.1% efficiency," *Applied Physics Letters,* vol. 107, no. 23, p. 233506, 2015.

[8] J. P. Hermans, R. v. Knippenberg, E. Kamp, W. J. M. Brok, P. Papet, B. Legradic and B. Strahm, "Inkjet printing for solar cell mass production on the pixdro jetx platform," in *Proceedings of 28th EU PVSEC*, 2013.

[9] J. Geissbuhler, S. D. Wolf, A. Faes, N. Badel, Q. Jeangros, A. Tomasi, L. Barraud, A. Descoeudres, M. Despeisse and C. Ballif, "Silicon Heterojunction Solar Cells With Copper-Plated Grid Electrodes: Status and Comparison with Silver Thick-Film Tequniques," *IEEE Journal of Photovoltaics,* vol. 4, no. 4, pp. 1055-1062, 2014.

[10] J. Heng, J. Fu, B. Kong, Y. Chae, W. Wang, Z. Xie, A. Reddy, K. Lam, C. Beitel, C. Liao, C. Erben, Z. Huang and Z. Xu, ">23% High-Efficiency Tunnel Oxide Junction Bifacial Solar Cell with Electroplated Cu Gridlines," *IEEE Journal of Photovoltaics,* vol. 5, no. 1, pp. 82-86, January 2015.

[11] J. Yu, J. Bian, W. Duan, Y. Liu, J. Shi, F. Meng and Z. Liu, "Tungsten doped indium oxide film: Ready for bifacial copper metallization of silicon heterojunction solar cell," *Solar Energy Materials and Solar Cells,* vol. 144, pp. 359-363, 2016.

[12] A. Goodrich, P. Hacke, Q. Wang, B. Sopori, R. Margolis, T. L. James and M. Woodhouse, "A wafer-based monocrystalline silicon photovoltaics road map: Utilizing knowntechnology improvement opportunities for further reductions in manufacturing costs," *Solar Energy Materials and Solar Cells,* vol. 114, pp. 110-135, 2013.

[13] P. A. Basore, "Understanding Manufacturing Cost Influence on Future Trends in Silicon Photovoltaics," *IEEE Journal of Photovoltaics,* vol. 4, no. 6, pp. 1477-1482, 2014.

[14] M. B. C. R. M. H. S. W. G. F. Feldmann, "A Passivated Rear Contact for High-Efficiency n-Type Silicon Solar Cells Enabling High Voc and FF>82%," in *28th European PV Solar Energy Conference and Exhibition*, Paris, France, 2013.

[15] M. Hutchins, "Improving n-type TOPCon Solar Cells," 9 September 2022. [Online]. Available: https://www.pv-magazine.com/2022/09/09/improving-n-type-topcon-solar-cells/.

[16] Y. Chen, D. Chen, C. Liu, Z. Wang, Y. Zou, Y. He, Y. Wang, L. Yuan, J. Gong, W. Lin, X. Zhang, Y. Yang, H. Shen, Z. Feng, P. Altermatt and P. Verlinden, "Mass Production of Industrial Tunnel Oxide Passivated Contacts (i-TOPCon) Silicon Solar Cells with Average Efficiency over 23% and modules over 345W," *Progress in Photovoltaics: Research and Applications,* vol. 27, no. 10, pp. 827-834, 2019.

[17] Y. Huang, Y. Ok, K. Madani, W. Choi, A. D. Upadhyaya, V. D. Upadhyaya and A. Rohatgi, "Fully Screen-printed Bifacial Large Area 22.6% N-type Si Solar Cell with Lightly Doped Ion-implanted Boron Emitter and Tunnel Oxide Passivated Rear Contact," *Solar Energy Materials and Solar Cells,* vol. 214, pp. 1-6, 2020.

[18] D. Bouhafs, A. Moussi, A. Chikouche and J. M. Ruiz, "Design and Simulation of Antireflection coating systems for optoelectronic devices: Application to Silicon Solar Cells," *Solar Energy Materials and Solar Cells,* vol. 52, no. 1, pp. 79-93, 1998.

[19] B. Hoex, J. Smidth, R. Bock, P. P. Altermatt, M. C. M. v. d. Sanden and W. M. M. Kessels, "Excellent Passivation of Highly Doped p-type Si Surfaces by the negative-charge-dielectric Al2O3," *Applied Physics Letters,* vol. 91, pp. 112107 1-3, 2007.

[20] J. Walter, M. Tranitz, M. Volk, C. Ebert and U. Eitner, "Multi-wire interconnection of busbar-free solar cells," *Energy Procedia,* vol. 55, pp. 380-388, 2014.

[21] B. Grubel, G. Cimiotti, V. Arya, B. Steinhauser and S. Kluska, "Plating Process for Bifacial TOPCon Solar Cells," in *9th Workshop on Metallization & Interconnection for Crystalline Silicon Solar Cells*, Virtual, 2020.

[22] A. Lennon, Y. Yao and S. Wenham, "Evolution of metal plating for silicon solar cell metallisation," *Progress in Photovoltaics: Research and Applications,* vol. 21, no. 7, pp. 1454-1468, 2012.

[23] S. B. Rane, T. Seth, G. J. Phatak and D. P. Amalnerkar, "Effect of inorganic binders on the properties of silver thick films," *Journal of Materials Science: Materials in Electronics,* vol. 15, pp. 103-106, 2004.

[24] Y. Shih, Y. Lin, J. You and F. Shi, "Screen-Printable Silver Pastes with Nanosized Glass Frits for Silicon Solar Cells," *Journal of Electronic Materials,* vol. 42, no. 3, pp. 410-416, 2013.

[25] C. Honsberg and S. Bowden, "PV Education," [Online]. Available: https://www.pveducation.org/.

[26] M. Mikolasek, M. Nemec, J. Kovac, M. Foti, C. Gerardi, G. Mannino, L. Valenti and S. Lombardo, "The influence of post-deposition annealing upon amorphous silicon/crystalline silicon heterojunction solar cells," *Materials Science and Engineering: B,* vol. 189, pp. 1-6, 2014.

[27] Y. Tsunomura, Y. Yoshimine, M. Taguchi, T. Baba, T. Kinoshita, H. Kanno, H. Sakata, E. Maruyama and M. Tanaka, "Twenty-two percent efficiency HIT solar cell," *Solar Energy Materials & Solar Cells,* vol. 93, pp. 670-673, 2009.

[28] D. Chen, L. Zhao, H. Diao, W. Zhang, G. Wang and W. Wang, "Choice of the low-temperature sintering Ag paste for a-Si:H/c-Si heterojunction solar cell based on characterizing the electrical performance," *Journal of Alloys and Compounds,* vol. 618, pp. 357-365, 2015.

[29] "Silver Prices - 100 Year Historical Chart," Macrotrends LLC, 2020. [Online]. Available: https://www.macrotrends.net/1470/historical-silver-prices-100-year-chart.

[30] "Copper Prices - 45 Year Historical Chart," Macrotrends LLC, 2020. [Online]. Available: https://www.macrotrends.net/1476/copper-prices-historical-chart-data.

[31] J. Ho, T. Dullweber, M. Fischer, S. Herritsch and J. Trube, "Main requirements for solar cells," in *Silicon Solar Cell Metallization and Module Technology*, T. Dullweber and L. Tous, Eds., London, The Institution of Engineering and Technology, 2021, pp. 23-28.

[32] "Mineral Commodity Summaries," US Geological Survey, 2022.

[33] W. Sun, *Development of Silver-Free Silicon Photovoltaic Solar Cells with all-Aluminum Electrodes,* Arizona State University, 2016.

[34] M. I. Hoffert, K. Caldeira, A. K. Jain, E. F. Haites, L. D. D. Harvey, S. D. Potter, M. E. Schlesinger, S. H. Schneider, R. G. Watts, T. M. L. Wigley and D. J. Wuebbles, "Energy implications of future stabilization of atmospheric CO2 content," *Nature,* vol. 395, no. 6705, pp. 881-884, 1998.

[35] "Demand for Silver Worldwide in 2017, by end use," Statista, 2017. [Online]. Available: https://www.statista.com/statistics/253345/global-silver-demand-by-purpose/.

[36] MicroChemicals, "Basics of Microstructuring," 2018. [Online]. Available: https://www.microchemicals.com/downloads/application_notes.html.

[37] J. Geissbuhler, A. Faes, A. Lachowicz, C. Ballif and M. Despeisse, "Metallization techniques and interconnnection schemes for high-efficiency silicon heterojunction PV," *Photovoltaics International,* vol. 37, pp. 61-69, 2017.

[38] D. Shin, H. Chung, H. Song, J. Lee, K. Kim and G. Kang, "Thermomechanical-stress-free interconnection of solar cells using a liquid metal," *Solar Energy Materials and Solar Cells,* vol. 180, pp. 10-18, 2018.

[39] M. Heimann, P. Klaerner, C. Luechinger, A. Mette, J. W. Mueller, M. Traeger, T. Barthel, O. Valentin and P. Wawer, "Ultrasonic Bonding of Aluminum Ribbons to Interconnect High-Efficiency Crystalline-Silicon Solar Cells," *Energy Procedia,* vol. 27, pp. 670-675, 2012.

[40] M. Hilali, J. Gee and P. Hacke, "Bow in screen-printed back-contact industrial silicon solar cells," *Solar Energy Materials and Solar Cells,* vol. 91, no. 13, pp. 1228-1233, 2007.

[41] S. Lagrange, S. H. Brongersma, M. Judelewicz, A. Saerens, I. Vervoort, E. Richard, R. Palmans and K. Maex, "Self-annealing characterization of electroplated copper films," *Microelectronic Engineering,* vol. 50, pp. 449-457, 2000.

[42] M. Stangl, M. Liptak, A. Fletcher, J. Acker, J. Thomas, H. Wendrock, S. Oswald and K. Wetzig, "Influence of initial microstructure and impurities on Cu room-temperature recrystallization (self-annealing)," *Microelectronic Engineering,* vol. 85, pp. 534-541, September 2008.

[43] J. W. Chen and A. G. Milnes, "Energy Levels in Silicon," *Annual Review of Materials Science,* vol. 10, no. 1, pp. 157-228, 1980.

[44] H. G. Grimmeiss, "Deep Level Impurities in Semiconductors," *Annual Review of Materials Science,* vol. 7, no. 1, pp. 341-376, 1977.

[45] S. Knack, "Copper-related defects in silicon," *Materials Science in Semiconductor Processing,* vol. 7, no. 3, pp. 125-141, 2004.

[46] J. Hernandez, K. Yoshikawa, A. Feltrin, N. Menou, N. Valckx, E. Assche, D. Schroos, K. Vandersmissen, H. Philipsen, J. Poortmans, D. Adachi, M. Yoshimi, T. Uto, H. Uzu, T. Kuchiyama, C. Allebe, N. Nakanishi, T. Terashita, T. Fujumoto, G. Koizumi and K. Yamam, "High Efficiency Silver-Free Heterojunction Silicon Solar Cell," *Japanese Journal of Applied Physics,* vol. 51, pp. 10NA04 1-3, 2012.

[47] A. Kim, H. Park, E. Choi, Y. Cui, S. Lee and S. Pyo, "Development of Electroless-Deposited Electrode in Heterojunction with Intrinsic Thin-Layer Solar Cell," *Israel Journal of Chemistry,* vol. 55, no. 10, pp. 1070-1074, 2015.

[48] R. Rohit, A. Rodofili, G. Cimiotti, J. Bartsch and M. Glatthaar, "Selective plating concept for silicon heterojunction solar cell metallization," *Energy Procedia,* vol. 124, pp. 901-906, 2017.

[49] T. Hatt, V. Mehta, J. Bartsch, S. Kluska, M. Jahn, D. Borchert and M. Glatthaar, "Novel Mask-less Plating Metallization Route for Bifacial Silicon Heterojunction Solar Cells," in *AIP Conference Proceedings*, 2018.

[50] T. Hatt, J. Bartsch, Y. Franzl, S. Kluska and M. Glatthaar, "Advances with resist-free copper plating approaches for metallization of silicon heterojunction solar cells," *AIP Conference Proceedings,* vol. 2156, no. 1, p. 020010, 2019.

[51] A. Khanna, K.-U. Ritzau, M. Kamp, A. Filipovic, C. Schmiga, M. Glatthaar, A. G. Aberle and T. Mueller, "Screen-printed masking of transparent conductive oxide layers for copper plating of silicon heterojunction cells," *Applied Surface Science,* vol. 349, pp. 880-886, May 2015.

[52] J. Yu, J. Li, Y. Zhao, A. Lambertz, T. Chen, W. Duan, W. Liu, X. Yang, Y. Huang and K. Ding, "Copper metallization of electrodes for silicon heterojunction solar cells: Process, reliability and challenges," *Solar Energy Materials and Solar Cells,* vol. 224, p. 110993, 2021.

[53] B. S. Richards, "Comparison of TiO2 and other dielectric coatings for buried-contact solar cells: a review," *Progress in Photovoltaics: Research and Applications,* vol. 12, no. 4, pp. 253-281, 2004.

[54] J. Yu, L. Zhang, T. Chen, J. Bian, J. Shi, F. Meng, Y. Huang and Z. Liu, "Dual-Function Light-Trapping: Selective Plating Mask of SiOx/SiNx Stacks for Silicon Heterojunction Solar Cells," *Solar RRL,* vol. 3, no. 3, pp. 1-7, 2019.

[55] G. Limodio, Y. D. Groot, G. V. Kuler, L. Mazzarella, Y. Zhao, P. Procel, G. Yang, O. Isabella and M. Zeman, "Copper-Plating Metallization With Alternative Seed Layers for c-Si Solar Cells Embedding Carrier-Selective Passivating Contacts," *IEEE Journal of Photovoltaics,* vol. 10, no. 2, pp. 372-382, 2020.

[56] J. Madden, S. Lafontaine and I. Hunter, "Fabrication by Electrodeposition: Building 3D Structures and Polymer Actuators," in *Proceedings of the Sixth International Symposium on Micro Machine and Human Science*, 1995.

[57] Z. Li, P. Hsiao, W. Zhang, R. Chen, Y. Yao, P. Papet and A. Lennon, "Patterning for Plated Heterojunction Cells," *Enregy Procedia,* vol. 67, pp. 76-83, April 2015.

[58] W. Späth, "Verfahren zur galvanischen Abscheidung einer Metallschicht auf der Oberfläche eines Halbleiterkörpers". Germany 1979.

[59] A. Mette, "New concepts for front side metallization of industrial silicon solar cells," 2007.

[60] A. Kale, E. Beese, T. Saenz, E. Warren, W. Nemeth, D. Young, A. Marshall, K. Florent, S. K. Kurinec and S. Agarwal, "Study of nickel silicide as a copper diffusion barrier in monocrystalline silicon solar cells," in *IEEE 43rd Photovoltaic Specialists Conference (PVSC)*, Portland, 2016.

[61] M. Raval, A. Joshi, S. Saseendran, S. Suckow, S. Saravanan, C. Solanki and A. Kottantharayil, *IEEE Journal of Photovoltaics,* vol. 5, no. 6, pp. 1554-1562, 2015.

[62] J. Karas, S. Kim, L. Michaelson, K. Munoz, T. Tyson and S. Bowden, "Electrical characterization of thermally-formed nickel silicide for nickel-copper plated solar cell contacts," in *IEEE 42nd Photovoltaic Specialist Conference (PVSC)*, 2015.

[63] M. J. Madou, Fundamentals of Microfabrication and Nanotechnology, Boca Raton: Taylor & Francis Group, 2012.

[64] M. Galiazzo, A. Voltan, E. Bortoletto, M. Zamuner, M. Martire, O. Borsato, M. Bertazzo and D. Tonini, "Fine Line Double Printing and Advanced Process Control for Cell Manufacturing," *Energy Procedia,* vol. 67, pp. 116-125, 2015.

[65] T. Young, K. Hee, A. Lennon, R. Egan, O. Wilkie and Y. Yao, "Design and characterization of an adhesion strength tester for evaluating metal contacts on silicon solar cells," in *IEEE 40th Photovoltaic Specialist Conference (PVSC)*, 2014.

[66] J. Wendt, M. Trager, R. Klengel, M. Petzold, D. Schade and R. Sykes, "Improved quality test method for solder ribbon interconnects on silicon solar cells," in *12th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems*, 2010.

[67] A. Mondon, M. N. Jawaid, J. Bartsch, M. Glatthaar and S. W. Glunz, "Microstructure analysis of the interface situation and adhesion of thermally formed nickel silicide for plated nickel–copper contacts on silicon solar cells," *Solar Energy Materials and Solar Cells,* vol. 117, pp. 209-213, 2013.

[68] J. Xu, W. Ren, Z. Lian, P. Yu and H. Yu, "A Review: Development of the Maskless Localized Electrochemical Deposition Technology," *The International Journal of*

Advanced Manufacturing Technology, vol. 110, no. 7-8, pp. 1731-1757, 27 August 2020.

[69] F. Wang, H. BIan and Y. Xiao, "Fabrication of micro-sized copper columns using localized electrochemical deposition with a 20um diameter micro anode," *ECS Journal of Solid State Science and Technology,* vol. 8.4, p. 223, 2019.

[70] Y. J. Ciou, Y. R. Hwang, J. C. Lin, S. J. Chen and Y. T. Tseng, "Ciou, Yong-Jie, et al. "Comparison of simulation and experimental results for the deposition orientation in localized electrochemical deposition," *Japanese Journal of Applied Physics,* vol. 57, no. 11, p. 117301, 2018.

[71] A. Jansson, G. Thornell and S. Johansson, "High resolution 3D microstructures made by localized electrodeposition of nickel," *Journal of the Electrochemical Society,* vol. 147, no. 5, pp. 1810-1817, 2000.

[72] F. Wang, H. Bian, F. Wang, J. Sun and W. Zhu, "Fabrication of Micro Copper Walls by Localized Electrochemical Deposition through the Layer by Layer Movement of a Micro Anode," *Journal of The Electrochemical Society,* vol. 164, no. 12, 2017.

[73] L. Hirt, S. Ihle, Z. Pan, L. Dorwling-Carter, A. Reiser, J. M. Wheeler, R. Spolenak, J. Voros and T. Zambelli, "Template-free 3D microprinting of metals using a force-controlled nanopipette for layer-by-layer electrodeposition," *Advanced Materials,* vol. 28, no. 12, pp. 2311-2315, 2016.

[74] F. Wang, H. Xiao and H. He, "Effects of applied potential and the initial gap between electrodes on localized electrochemical deposition of micrometer copper columns," *Scientific Reports,* vol. 6, no. 1, pp. 1-8, 2016.

[75] A. Fell, K. McIntosh, P. Altermatt, G. Janssen, R. Stangl, A. Ho-Baillie, H. Steinkemper, J. Greulich, M. Muller, B. Min and e. al., "Input Parameters for the Simulation of Silicon Solar Cells in 2014," *IEEE Journal of Photovoltaics,* vol. 5, no. 4, pp. 1250-1263, 2015.

[76] J. Wong, "Griddler: Intelligent computer aided design of complex solar cell metallization patterns," in *IEEE 39th Photovoltaic Specialists Conference (PVSC)*, 2013.

[77] C. S. Lin, C. Y. Lee, J. H. Yang and Y. S. Huang, "Improved copper microcolumn fabricated by localized electrochemical deposition," *Electrochemical and Solid State Letters,* vol. 8, no. 9, pp. C125-129, 2005.

[78] R. A. Said, "Microfabrication by localized electrochemical deposition: experimental investigation and theoretical modelling," *Nanotechnology,* vol. 14, no. 5, p. 523, 2003.

[79] D. Pletcher, A First Course in Electrode Processes, 2 ed., Cambridge: The Royal Society of Chemistry, 2009.

[80] H. Xiao, P. Zeng, X. Ren and F. Wang, "Three-dimensional microfabrication of copper column by localized electrochemical deposition," in *17th International Conference on Electronic Packaging Technology (ICEPT)*, 2016.

[81] F. Wang, J. Sun, D. Liu, Y. Wang and W. Zhu, "Effect of voltage and gap on micro-nickel-column growth patterns in localized electrochemical deposition," *Journal of The Electrochemical Society,* vol. 164, no. 6, pp. D297-301, 2017.

[82] J. C. Lin, T. K. Chang, J. H. Yang, Y. S. Chen and C. L. Chuang, "Localized electrochemical deposition of micrometer copper columns by pulse plating," *Electrochimica Acta,* vol. 55, no. 6, pp. 1888-1894, 2010.

[83] S. K. Seol, A. R. Pyun, Y. Hwu, G. Margaritondo and J. H. Je, "Localized electrochemical deposition of copper monitored using real-time x-ray microradiography," *Advanced Functional Materials,* vol. 15, no. 6, pp. 934-937, 2005.

[84] C.-Y. Lee, C.-S. Lin and B.-R. Lin, "Localized electrochemical deposition process improvement by using different anodes and deposition directions," *Journal of Micromechanics and Microengineering,* vol. 18, no. 10, pp. 1-8, 2008.

[85] M. Schlesinger and M. Paunovic, Modern Electroplating, 5 ed., Hoboken: John Wiley & Sons, 2010.

[86] S. K. Seol, J. T. Kim, J. H. Je, Y. Hwu and G. Margaritondo, "Fabrication of Freestanding Metallic Micro Hollow Tubes by Template-Free Localized Electrochemical Deposition," *Electrochemical and Solid State Letters,* vol. 10, no. 5, pp. 44-46, 2007.